PVG610A
Data Sheet

PVG610A_DSH_002_I3

Provigent

Intelligent Silicon for Broadband Wireless

Revision History

Date Released	Release	Reason for Revision	Comments
21-June-2007	002-F	1. Pin list in chapter 2.2: E6 SPARE 0 is corrected to A6 SPARE 0 2. Chapter 8.1 Absolute Maximum Rating: Junction temperature is -40 to 125°C 3. Updated fig. 106 4. Dual DAC DC Specification, Power dissipation update in 6.4.3.2 5. Added section 5.4 System Clock Mode 6. Timing diagrams and tables in chapter 6 updated	
18-July-2007	002-F1	1. Number of clock cycles between Tx/Rx Sync and Tx/Rx ACM is changed to 2 (chapter 6.2.6) 2. Updated SPI Diagram 6.3.2	
19-sep-2007	002-G	1. Max sampling rate of Envelope ADC corrected to 80Msamples/sec (chapter 6.4.4) 2. Power consumption values added in 8.5 3. Description for Watch-dog mechanism added in 3.7.3	
18-oct-2007	002-G1	1. LIU power consumption update (8.5.2) 2. Update Thermal resistance parameter	
23-Dec-2007	002-H	1. Signal direction of AK15 corrected to Output (2.2) 2. XPIC slave power consumption added (8.5.1) 3. Location of RX_ACM signal corrected (6.2.6) 4. TBI Interface is removed 5. AFE spec updated (6.4) 6. HS mode in I2C removed (6.3.3)	
02-April-2008	002-H2	1. Updating LIU power consumption (8.5.3) 2. MRC configuration removed (6.6)	
23-June-2008	002-H4	1. Remove Boot process description (5.3.1). 2. Rise/fall time parameters added to 6.2.2.1. 3. Update PDH MCLK reference clock frequency.	
10-Nov-2008	002-H5	1. Max DDS CLK frequency is 112MHz (6.2.6) 2. Update Figure 76 3. Update operating conditions for VDD1P2 (8.2)	

		4. Rx of Tx block added (3.6.4.9) 5. Update Figure 74 (TOH timing diagram) 6. Update Figure 98 (HDLC timing diagram)	
01-July-2009	002-I	1. Update Figure 98 (HDLC timing diagram) 2. RX_UC signal is active high (6.5) 3. SPI timing (6.3.2) 4. Update power up sequence (8.3) 5. PDH LIU spec update (6.2.1) 6. Added I/O drive currents (2)	
13-Sep-2009	002-I1	Name change only; PVG610 to PVG610A	
14-Sep_2009	002-I2	Table 56: Protection Interface Timing – IN_STB is changed to OUT-STB and correction a typo	
5-Dec-2010	002-I3	"Configurable" is removed in paragraph 6.3.5 T_{CLK} and T_{PD} are updated in Table 40	

International

Provigent Ltd.

4 Shenkar St. Herzlia
POB 2168, 46120, Israel
Tel: +972 (9)950-5434
Fax: +972 (9)950-5683

USA

Provigent Inc.

3333 Bowers Ave.
Santa Clara, CA 95054-2913
Tel: (408) 701-2250
Fax: (408) 715-0188

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1 Introduction

1.1 PVG610A Family Overview

The PVG610A is a family of broadband Point to Point wireless System-on-Chip devices. It provides an unparallel level of integration for fixed broadband wireless systems targeted for cellular access networks, fixed wireless transmission links, and private wireless networks. It is a highly integrated mixed signal device that provides a complete processing chain from user data interfaces to analog baseband or IF signal. This System-on-a-chip includes a high capacity, robust QAM modem for point-to-point microwave and mm-wave radio systems.

The drawing below illustrates the PVG610A general architecture

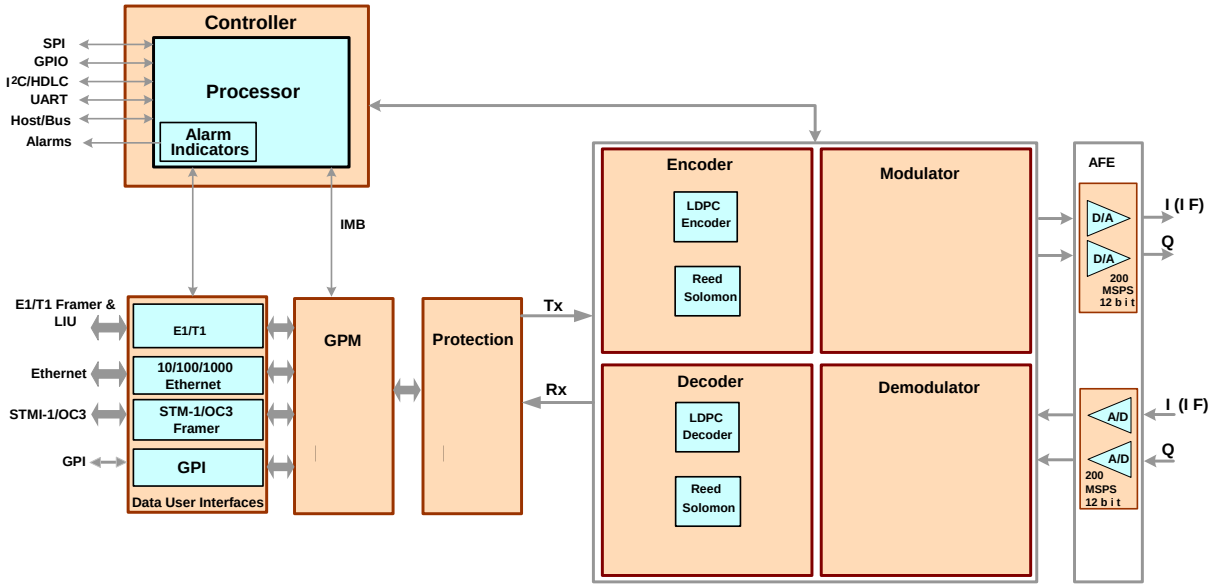


Figure 1: PVG610A General Architecture

The diagram above shows the path of user's data from the standard interface connection to the transmitted airframe. And the path from the received airframe to the standard interface connection.

PVG610A supports four main data streams, three standard data protocols; STM-1/OC3, E1/T1 and Ethernet 10/100/1000 and a General Purpose Interface for user's unique requirement. Other interfaces are described in the Functional Description. It includes TOH for injecting data into the STM-1/OC3 stream and service streams; EOW and OMI.

The General Purpose Multiplexer (GPM) manages and streamlines all concurrently incoming data toward the airframe. The protection block diversifies traffic upon link failure report. The serial data stream enters the modem block in which it is encoded in LDPC or Reed Solomon algorithm and then modulated. The digital streams in an airframe format pass through the Analog Front End (AFE) block in which it is converted to analog, sending the 'I' and 'Q' IF signals.

In the receive direction IF analog signals, (I) and (Q), are converted to digital in the AFE unit and passed to the modem for demodulation and decoding. The signal then passes through the protection block to the GPM in which it is forwarded to the appropriate used interface.

This document describes a superset of features and capabilities supported in the PVG610A family. Availability of specific features and capabilities depends on the licensing agreement with Provigent.

1.2 PVG610X Vs. PVG610A

The PVG610A device supports all features described in this document except for the XPIC mode.

The PVG610X device supports all features described in this document except for the number of E1/T1/J1 ports. The PVG610X supports only two E1/T1/J1 ports, and not 21 ports as in the PVG610.

In XPIC application four PVG610X devices are used; two are used as Master devices and two are used as Slave devices. For additional details see section 5.2.3 .

2 Pin Description

This document provides a comprehensive description of the PVG610A functionalities. To allow for quick access and reference to the pin layout and signal list they are located at the very beginning of the document.

This chapter contains the pin layout and list of signals of the PVG610A and XPIC version.

2.1 Pin Layout

The four diagrams below illustrate the pin layout of PVG610A and PVG610X (XPIC). The modules have a matrix of 34 H x 34 V pins layout. Each diagram is split to 17 H x 34 V pin layout to allow for visibility of the signal names.

There are a total of 680 balls in the PVG610A/PVG610X package, grouped as shown in the table below; Functional, Power, Thermal and Not-Connected.

	Functional	Power	N.C.
PVG610A	361	319	0
PVG610X	330	319	31

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17
A	VSS	VSS	SYS_CLK_N	SYS_CLK_P	VSS	SPARE_0	DAC_VSS	OUT_I_P	OUT_I_N	DAC_VSS	DAC_VSS	OUT_Q_N	OUT_Q_P	DAC_VSS	DAC_VSS	ENV_IN_N	ENV_IN_P
B	VSS	VSS	VSS	VSS	VSS	SPARE_1	DAC_VSS	DAC_VSS	DAC_VSS	DAC_VSS	IREF	DAC_VSS	DAC_VSS	DAC_VSS	DAC_VSS	ENV_VCM	DAC_VSS
C	LIU_VDD3P3	VSS	LIU_VDD3P3	VSS	VSS	SPARE_2	DAC_VSS	DAC_VDD3P3	DAC_VDD3P3	DAC_VDD3P3	DAC_VDD3P3	DAC_VDD3P3	DAC_VDD3P3	DAC_VDD3P3	DAC_VDD1P2	DAC_VDD1P2	DAC_VDD1P2
D	RRING_20	RTIP_20	LIU_VDD3P3	TRING_20	TTIP_20	VSS	DAC_VSS	DAC_VDD3P3	DAC_CLK_VSS	DAC_CLK_VDD1P2	DAC_VSS	DAC_VDD3P3	DAC_VSS	DAC_VDD3P3	DAC_VSS	DAC_VDD1P2	DAC_VSS
E	RRING_19	RTIP_19	VSS	TRING_19	TTIP_19	VSS	DAC_VSS	DAC_VSS	DAC_CLK_N	DAC_CLK_P	DAC_VDD3P3	DAC_VSS	DAC_VDD3P3	DAC_VSS	DAC_VDD1P2	DAC_VSS	DAC_VDD1P2
F	RRING_18	RTIP_18	LIU_VDD3P3	TRING_18	TTIP_18												
G	R_REF_17	VSS	LIU_VDD3P3	VSS	LIU_VDD3P3												
H	RRING_17	RTIP_17	LIU_VDD3P3	TRING_17	TTIP_17												
J	RRING_16	RTIP_16	VSS	TRING_16	TTIP_16												
K	RRING_15	RTIP_15	LIU_VDD3P3	TRING_15	TTIP_15												
L	VSS	VSS	LIU_VDD3P3	VSS	LIU_VDD3P3												
M	RRING_14	RTIP_14	LIU_VDD3P3	TRING_14	TTIP_14												
N	RRING_13	RTIP_13	VSS	TRING_13	TTIP_13								PLL_VSSA	SYS_CLK_VSS	SYS_CLK_VDD1P2	VDD1P2	VDD1P2
P	RRING_12	RTIP_12	LIU_VDD3P3	TRING_12	TTIP_12								PLL_VDDA1P2	VSS	VSS	VSS	VSS
R	R_REF_12	VSS	LIU_VDD3P3	VSS	LIU_VDD3P3								VDD1P2	VSS	VSS	VSS	VSS
T	RRING_11	RTIP_11	LIU_VDD3P3	TRING_11	TTIP_11								VDD1P2	VSS	VSS	VSS	VSS
U	RRING_10	RTIP_10	VSS	TRING_10	TTIP_10								VDD1P2	VSS	VSS	VSS	VSS
V	RRING_9	RTIP_9	LIU_VDD3P3	TRING_9	TTIP_9								VDD1P2	VSS	VSS	VSS	VSS
W	VSS	VSS	LIU_VDD3P3	VSS	LIU_VDD3P3								VDD1P2	VSS	VSS	VSS	VSS
Y	TTIP_8	TRING_8	LIU_VDD3P3	RTIP_8	RRING_8								VDD1P2	VSS	VSS	VSS	VSS
AA	TTIP_7	TRING_7	VSS	RTIP_7	RRING_7								VDD1P2	VSS	VSS	VSS	VSS
AB	TTIP_6	TRING_6	LIU_VDD3P3	RTIP_6	RRING_6								VDD1P2	VDD1P2	VDD1P2	VDD1P2	VDD1P2
AC	VSS	VSS	LIU_VDD3P3	VSS	LIU_VDD3P3												
AD	TTIP_5	TRING_5	LIU_VDD3P3	RTIP_5	RRING_5												
AE	TTIP_4	TRING_4	VSS	RTIP_4	RRING_4												
AF	TTIP_3	TRING_3	LIU_VDD3P3	RTIP_3	RRING_3												
AG	VSS	VSS	LIU_VDD3P3	VSS	LIU_VDD3P3												
AH	TTIP_2	TRING_2	LIU_VDD3P3	RTIP_2	RRING_2												
AJ	TTIP_1	TRING_1	VSS	RTIP_1	RRING_1												
AK	TTIP_0	TRING_0	LIU_VDD3P3	RTIP_0	RRING_0	VSS	MII_CRS	MII_COL	STM1_B_RX_D_IN	MII_TBI_62_RX_C	STM1_B_RX_D_OUT	STM1_B_TX_SER_C	STM1_B_TX_FP	STM1_B_TX_D_IN	STM1_B_TX_D_OUT	GPIO_0	GPIO_1
AL	R_REF_0	VSS	LIU_VDD3P3	VSS	VSS	MII_MDIO	VDD3P3	MII_RXD_4	VSS	MII_TX_ER	VDD3P3	MII_TXD_4	VSS	HOST_ADDR_10	VDD3P3	GPIO_9	GPIO_11
AM	VSS	ACLK	VSS	MCLK	DFT_TEST	MII_MDC	MII_RXD_1	MII_RXD_5	MII_RXD_7	MII_RX_CLK	MII_TXD_7	MII_TXD_3	MII_TXD_1	HOST_ADDR_11	I2C_SCL	I2C_SDA	SPI_M_CS_0
AN	VSS	VSS	JTAG_TDI	JTAG_TRST	JTAG_SEL	VSS	MII_RXD_2	VDD3P3	MII_RX_DV	VSS	MII_TXD_6	VDD3P3	MII_TXD_0	VSS	OMI_TXD	OMI_RXD	SPI_M_DI
AP	VSS	VDD3P3	VDD3P3	JTAG_TMS	JTAG_TCK	JTAG_TDO	MII_RXD_0	MII_RXD_3	MII_RXD_6	MII_RX_ER	MII_TX_EN	MII_TXD_5	MII_TXD_2	MII_TX_CLK	OMI_TCLK	OMI_RCLK	SPI_M_CLK
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17

Figure 2: PVG610A Pin Layout 1-17 (Top View)

18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	
DAC_VSS	ADC_VSS	BB_IN_Q_P	BB_IN_Q_N	ADC_VSS	ADC_VSS	BB_IN_I_N	BB_IN_I_P	ADC_VSS	ADC_VSS	MADDR_2	MADDR_6	MADDR_10	MADDR_8	VDD3P3	VDD3P3	VDD3P3	A
DAC_VSS	ADC_VSS	VCM_Q	ADC_VSS	ADC_VSS	ADC_VSS	VCM_I	ADC_VSS	ADC_VSS	ADC_VSS	MADDR_3	VSS	MADDR_9	MCLKOUT	MADDR_7	VDD3P3	VSS	B
DAC_VDD1P2	ADC_VDD3P3	ADC_VDD1P2	ADC_VDD1P2	ADC_VDD1P2	ADC_VDD1P2	ADC_VDD1P2	ADC_VDD1P2	ADC_VSS	RF_MUTE	MADDR_4	MADDR_5	MADDR_0	VDD3P3	MADDR_11	MDATA_8	VSS	C
DAC_VDD1P2	ADC_VSS	IF_IN_P	ADC_VSS	ADC_CLK_VSS	ADC_CLK_VDD1P2	ADC_VSS	ADC_VSS	TR_SWITCH	SPI_M2_CS_0	SPI_M2_DI	MADDR_1	MDQMOUT_1	MADDR_14	MADDR_13	VSS	MFBCLKIN	D
DAC_VSS	ADC_VSS	IF_IN_N	ADC_VSS	ADC_CLK_N	ADC_CLK_P	ADC_VSS	LNA_PD	AGC_PWM	SPI_M2_DO	SPI_M2_CLK	MADDR_12	MCSOUT	VSS	MDATA_7	MDATA_9	MDATA_10	E
												MRASOUT	MDATA_11	MDATA_6	VDD3P3	MDATA_5	F
												MCASOUT	VDD3P3	MDATA_4	MDATA_12	MDATA_13	G
												MWEOUT	MDATA_14	MDATA_3	VSS	MDATA_2	H
												MDQMOUT_0	VSS	MDATA_15	MDATA_1	MDATA_0	J
												TEST_0	TEST_1	TEST_16	VDD3P3	TEST_17	K
												TEST_2	VDD3P3	TEST_3	TEST_18	TEST_19	L
												TEST_4	TEST_5	TEST_20	VSS	TEST_21	M
VDD1P2	VDD1P2	VDD1P2	VDD1P2	VDD1P2								TEST_6	VSS	TEST_7	TEST_22	TEST_23	N
VSS	VSS	VSS	VSS	VDD1P2								TEST_8	TEST_9	TEST_24	VDD3P3	TEST_25	P
VSS	VSS	VSS	VSS	VDD1P2								TEST_10	VDD3P3	TEST_11	TEST_26	TEST_27	R
VSS	VSS	VSS	VSS	VDD1P2								TEST_12	TEST_13	TEST_28	VSS	TEST_29	T
VSS	VSS	VSS	VSS	VDD1P2								TEST_14	VSS	TEST_15	TEST_30	TEST_31	U
VSS	VSS	VSS	VSS	VDD1P2								HOST_DATA_7	HOST_DATA_6	HOST_DATA_5	VDD3P3	HOST_CS	V
VSS	VSS	VSS	VSS	VDD1P2								HOST_DATA_15	VDD3P3	XPIC_HOST_CS_N	HOST_DATA_14	HOST_DATA_3	W
VSS	VSS	VSS	VSS	VDD1P2								HOST_DATA_9	HOST_DATA_11	HOST_DATA_10	VSS	HOST_DATA_2	Y
VSS	VSS	VSS	VSS	VDD1P2								HOST_DATA_1	VSS	HOST_ADDR_0	HOST_WE	HOST_OE	AA
VDD1P2	VDD1P2	VDD1P2	VDD1P2	VDD1P2								HOST_DATA_12	HOST_DATA_8	HOST_DATA_13	VDD3P3	HOST_DATA_4	AB
												TX_SYNC	VDD3P3	HOST_DPRAM_IRQ	HOST_INT	HOST_DATA_0	AC
												TX_ACM	TX_DATA_6	TX_DATA_7	VSS	TX_DATA_5	AD
												TX_AF	VSS	TX_DATA_3	TX_DATA_4	TX_DATA_2	AE
												TX_WE	TX_DATA_0	TX_DATA_1	VDD3P3	TX_AE	AF
												RX_AE	VDD3P3	RX_ACM	RX_UNCOR	TX_CLK	AG
												RX_RE	RX_DATA_7	RX_CLK	VSS	STM1_A_RX_CLK	AH
												RX_SYNC	VSS	RX_DATA_5	RX_DATA_6	RX_DATA_4	AJ
GPIO_2	GPIO_3	GPIO_8	GPIO_12	RXP_IN_DATA_3	RXP_IN_DATA_2	RXP_IN_STB	RXP_IN_SYNC	RXP_IN_DATA_1	RXP_IN_DATA_0	DDS3	STM1_A_RX_LOSS	VDD3P3	RX_DATA_3	RX_DATA_2	VDD3P3	STM1_A_VCXO_CLK	AK
GPIO_13	VSS	GPIO_14	WD	VDD3P3	RXP_IN_DATA_6	VSS	RXP_IN_DATA_5	VDD3P3	RXP_IN_DATA_4	VSS	DDS4	STM1_A_TX_FP	VDD3P3	RX_DATA_0	STM1_A_VCXO_PWM	RX_DATA_1	AL
GPIO_15	GPIO_4	GPIO_5	GPIO_10	TXP_IN_DATA_3	TXP_IN_DATA_2	RXP_IN_UC	TXP_IN_DATA_1	RXP_IN_DATA_7	TXP_IN_DATA_0	SYS_CLK_OUT	STM1_A_TX_D_OUT	STM1_A_TX_D_IN	STM1_A_RX_D_IN	VDD3P3	STM1_A_RX_FP	VSS	AM
VDD3P3	GPIO_6	GPIO_7	VSS	AIRLOSS	VDD3P3	TXP_IN_DATA_5	VSS	TXP_IN_DATA_4	VDD3P3	EOW_FP	EOW_RDATA	VSS	STM1_A_RX_D_OUT	STM1_REF_CLK	VDD3P3	VDD3P3	AN
SPI_M_DO	UART_RXD	UART_TXD	NRESET_OUT	NRESET	CPU_NRESET	TXP_IN_DATA_7	TXP_IN_DATA_6	TXP_IN_STB	TXP_IN_SYNC	EOW_CLK	EOW_TDATA	STM1_A_TX_SER_C	STM1_A_RX_SER_C	RX_AF	VDD3P3	VDD3P3	AP
18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	

Figure 3: PVG610A Pin Layout 18-34 (Top View)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17
A	VSS	VSS	SYS_CLK_N	SYS_CLK_P	VSS	SPARE_0	DAC_VSS	OUT_I_P	OUT_I_N	DAC_VSS	DAC_VSS	OUT_Q_N	OUT_Q_P	DAC_VSS	DAC_VSS	ENV_IN_N	ENV_IN_P
B	VSS	VSS	VSS	VSS	VSS	SPARE_1	DAC_VSS	DAC_VSS	DAC_VSS	DAC_VSS	IREF	DAC_VSS	DAC_VSS	DAC_VSS	DAC_VSS	ENV_VCM	DAC_VSS
C	LIU_VDD3P3	VSS	LIU_VDD3P3	VSS	VSS	SPARE_2	DAC_VSS	DAC_VDD3P3	DAC_VDD3P3	DAC_VDD3P3	DAC_VDD3P3	DAC_VDD3P3	DAC_VDD3P3	DAC_VDD3P3	DAC_VDD1P2	DAC_VDD1P2	DAC_VDD1P2
D	NC	NC	LIU_VDD3P3	NC	NC	VSS	DAC_VSS	DAC_VDD3P3	DAC_CLK_VSS	DAC_CLK_VDD1P2	DAC_VSS	DAC_VDD3P3	DAC_VSS	DAC_VDD3P3	DAC_VSS	DAC_VDD1P2	DAC_VSS
E	NC	NC	VSS	NC	NC	VSS	DAC_VSS	DAC_VSS	DAC_CLK_N	DAC_CLK_P	DAC_VDD3P3	DAC_VSS	DAC_VDD3P3	DAC_VSS	DAC_VDD1P2	DAC_VSS	DAC_VDD1P2
F	NC	NC	LIU_VDD3P3	NC	NC												
G	NC	VSS	LIU_VDD3P3	VSS	LIU_VDD3P3												
H	NC	NC	LIU_VDD3P3	NC	NC												
J	TIMO_MU_5	TIMO_MU_6	VSS	ERRO_7	ERRO_8												
K	TIMO_GET	TIMO_MU_4	LIU_VDD3P3	ERRO_4	ERRO_5												
L	VSS	VSS	LIU_VDD3P3	VSS	LIU_VDD3P3												
M	TIMO_CALC	TIMO_MU_3	LIU_VDD3P3	ERRO_PILOT	ERRO_2												
N	TIM_GET_OUT	TIMO_MU_2	VSS	ERRO_STROBE	ERRO_0								PLL_VSSA	SYS_CLK_VSS	SYS_CLK_VDD1P2	VDD1P2	VDD1P2
P	TIMO_MU_0	TIMO_MU_1	LIU_VDD3P3	ERRO_9	ERRO_6								PLL_VDDA1P2	VSS	VSS	VSS	VSS
R	NC	VSS	LIU_VDD3P3	VSS	LIU_VDD3P3								VDD1P2	VSS	VSS	VSS	VSS
T	SYMI_21	SYMI_22	LIU_VDD3P3	SYMI_23	ERRO_3								VDD1P2	VSS	VSS	VSS	VSS
U	SYMI_18	SYMI_19	VSS	SYMI_20	ERRO_1								VDD1P2	VSS	VSS	VSS	VSS
V	SYMI_15	SYMI_16	LIU_VDD3P3	SYMI_17	SYMI_0								VDD1P2	VSS	VSS	VSS	VSS
W	VSS	VSS	LIU_VDD3P3	VSS	LIU_VDD3P3								VDD1P2	VSS	VSS	VSS	VSS
Y	SYMI_3	SYMI_14	LIU_VDD3P3	SYMI_13	SYMI_STROBE								VDD1P2	VSS	VSS	VSS	VSS
AA	SYMI_2	SYMI_12	VSS	SYMI_11	SYMI_10								VDD1P2	VSS	VSS	VSS	VSS
AB	SYMI_1	SYMI_9	LIU_VDD3P3	SYMI_8	SYMI_7								VDD1P2	VDD1P2	VDD1P2	VDD1P2	VDD1P2
AC	VSS	VSS	LIU_VDD3P3	VSS	LIU_VDD3P3												
AD	SYMI_6	SYMI_5	LIU_VDD3P3	SYMI_4	NC												
AE	NC	NC	VSS	NC	NC												
AF	NC	NC	LIU_VDD3P3	NC	NC												
AG	VSS	VSS	LIU_VDD3P3	VSS	LIU_VDD3P3												
AH	NC	NC	LIU_VDD3P3	NC	NC												
AJ	TTIP_1	TRING_1	VSS	RTIP_1	RRING_1												
AK	TTIP_0	TRING_0	LIU_VDD3P3	RTIP_0	RRING_0	VSS	MII_CRS	MII_COL	STM1_B_RX_D_IN	MII_TBI_62_RX_C	STM1_B_RX_D_OUT	STM1_B_TX_SER_C	STM1_B_TX_FP	STM1_B_TX_D_IN	STM1_B_TX_D_OUT	GPIO_0	GPIO_1
AL	R_REF_0	VSS	LIU_VDD3P3	VSS	VSS	MII_MDIO	VDD3P3	MII_RXD_4	VSS	MII_TX_ER	VDD3P3	MII_TXD_4	VSS	HOST_ADDR_10	VDD3P3	GPIO_9	GPIO_11
AM	VSS	ACLK	VSS	MCLK	DFT_TEST	MII_MDC	MII_RXD_1	MII_RXD_5	MII_RXD_7	MII_RX_CLK	MII_TXD_7	MII_TXD_3	MII_TXD_1	HOST_ADDR_11	I2C_SCL	I2C_SDA	SPI_M_CS_0
AN	VSS	VSS	JTAG_TDI	JTAG_TRST	JTAG_SEL	VSS	MII_RXD_2	VDD3P3	MII_RX_DV	VSS	MII_TXD_6	VDD3P3	MII_TXD_0	VSS	OMI_TXD	OMI_RXD	SPI_M_DI
AP	VSS	VDD3P3	VDD3P3	JTAG_TMS	JTAG_TCK	JTAG_TDO	MII_RXD_0	MII_RXD_3	MII_RXD_6	MII_RX_ER	MII_TX_EN	MII_TXD_5	MII_TXD_2	MII_TX_CLK	OMI_TCLK	OMI_RCLK	SPI_M_CLK
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17

Figure 4: PVG610X (XPIC) Pin Layout 1-17 (Top View)

18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	
DAC_VSS	ADC_VSS	BB_IN_Q_P	BB_IN_Q_N	ADC_VSS	ADC_VSS	BB_IN_I_N	BB_IN_I_P	ADC_VSS	ADC_VSS	MADDR_2	MADDR_6	MADDR_10	MADDR_8	VDD3P3	VDD3P3	VDD3P3	A
DAC_VSS	ADC_VSS	VCM_Q	ADC_VSS	ADC_VSS	ADC_VSS	VCM_I	ADC_VSS	ADC_VSS	ADC_VSS	MADDR_3	VSS	MADDR_9	MCLKOUT	MADDR_7	VDD3P3	VSS	B
DAC_VDD1P2	ADC_VDD3P3	ADC_VDD1P2	ADC_VDD1P2	ADC_VDD1P2	ADC_VDD1P2	ADC_VDD1P2	ADC_VDD1P2	ADC_VSS	RF_MUTE	MADDR_4	MADDR_5	MADDR_0	VDD3P3	MADDR_11	MDATA_8	VSS	C
DAC_VDD1P2	ADC_VSS	IF_IN_P	ADC_VSS	ADC_CLK_VSS	ADC_CLK_VDD1P2	ADC_VSS	ADC_VSS	TR_SWITCH	SPI_M2_CS_0	SPI_M2_DI	MADDR_1	MDQMOUT_1	MADDR_14	MADDR_13	VSS	MFBCLKIN	D
DAC_VSS	ADC_VSS	IF_IN_N	ADC_VSS	ADC_CLK_N	ADC_CLK_P	ADC_VSS	LNA_PD	AGC_PWM	SPI_M2_DO	SPI_M2_CLK	MADDR_12	MCSOUT	VSS	MDATA_7	MDATA_9	MDATA_10	E
												MRASOUT	MDATA_11	MDATA_6	VDD3P3	MDATA_5	F
												MCASOUT	VDD3P3	MDATA_4	MDATA_12	MDATA_13	G
												MWEOUT	MDATA_14	MDATA_3	VSS	MDATA_2	H
												MDQMOUT_0	VSS	MDATA_15	MDATA_1	MDATA_0	J
												TEST_0	TEST_1	TEST_16	VDD3P3	TEST_17	K
												TEST_2	VDD3P3	TEST_3	TEST_18	TEST_19	L
												TEST_4	TEST_5	TEST_20	VSS	TEST_21	M
VDD1P2	VDD1P2	VDD1P2	VDD1P2	VDD1P2								TEST_6	VSS	TEST_7	TEST_22	TEST_23	N
VSS	VSS	VSS	VSS	VDD1P2								TEST_8	TEST_9	TEST_24	VDD3P3	TEST_25	P
VSS	VSS	VSS	VSS	VDD1P2								TEST_10	VDD3P3	TEST_11	TEST_26	TEST_27	R
VSS	VSS	VSS	VSS	VDD1P2								TEST_12	TEST_13	TEST_28	VSS	TEST_29	T
VSS	VSS	VSS	VSS	VDD1P2								TEST_14	VSS	TEST_15	TEST_30	TEST_31	U
VSS	VSS	VSS	VSS	VDD1P2								HOST_DATA_7	HOST_DATA_6	HOST_DATA_5	VDD3P3	HOST_CS	V
VSS	VSS	VSS	VSS	VDD1P2								HOST_DATA_15	VDD3P3	XPIC_HOST_CS_N	HOST_DATA_14	HOST_DATA_3	W
VSS	VSS	VSS	VSS	VDD1P2								HOST_DATA_9	HOST_DATA_11	HOST_DATA_10	VSS	HOST_DATA_2	Y
VSS	VSS	VSS	VSS	VDD1P2								HOST_DATA_1	VSS	HOST_ADDR_0	HOST_WE	HOST_OE	AA
VDD1P2	VDD1P2	VDD1P2	VDD1P2	VDD1P2								HOST_DATA_12	HOST_DATA_8	HOST_DATA_13	VDD3P3	HOST_DATA_4	AB
												TX_SYNC	VDD3P3	HOST_DPRAM_IRQ	HOST_INT	HOST_DATA_0	AC
												TX_ACM	TX_DATA_6	TX_DATA_7	VSS	TX_DATA_5	AD
												TX_AF	VSS	TX_DATA_3	TX_DATA_4	TX_DATA_2	AE
												TX_WE	TX_DATA_0	TX_DATA_1	VDD3P3	TX_AE	AF
												RX_AE	VDD3P3	RX_ACM	RX_UNCOR	TX_CLK	AG
												RX_RE	RX_DATA_7	RX_CLK	VSS	STM1_A_RX_CLK	AH
												RX_SYNC	VSS	RX_DATA_5	RX_DATA_6	RX_DATA_4	AJ
GPIO_2	GPIO_3	GPIO_8	GPIO_12	RXP_IN_DATA_3	RXP_IN_DATA_2	RXP_IN_STB	RXP_IN_SYNC	RXP_IN_DATA_1	RXP_IN_DATA_0	DDS3	STM1_A_RX_LOSS	VDD3P3	RX_DATA_3	RX_DATA_2	VDD3P3	STM1_A_VCXO_CLK	AK
GPIO_13	VSS	GPIO_14	WD	VDD3P3	RXP_IN_DATA_6	VSS	RXP_IN_DATA_5	VDD3P3	RXP_IN_DATA_4	VSS	DDS4	STM1_A_TX_FP	VDD3P3	RX_DATA_0	STM1_A_VCXO_PWM	RX_DATA_1	AL
GPIO_15	GPIO_4	GPIO_5	GPIO_10	TXP_IN_DATA_3	TXP_IN_DATA_2	RXP_IN_UC	TXP_IN_DATA_1	RXP_IN_DATA_7	TXP_IN_DATA_0	SYS_CLK_OUT	STM1_A_TX_D_OUT	STM1_A_TX_D_IN	STM1_A_RX_D_IN	VDD3P3	STM1_A_RX_FP	VSS	AM
VDD3P3	GPIO_6	GPIO_7	VSS	AIRLOSS	VDD3P3	TXP_IN_DATA_5	VSS	TXP_IN_DATA_4	VDD3P3	EOW_FP	EOW_RDATA	VSS	STM1_A_RX_D_OUT	STM1_REF_CLK	VDD3P3	VDD3P3	AN
SPI_M_DO	UART_RXD	UART_TXD	NRESET_OUT	NRESET	CPU_NRESET	TXP_IN_DATA_7	TXP_IN_DATA_6	TXP_IN_STB	TXP_IN_SYNC	EOW_CLK	EOW_TDATA	STM1_A_TX_SERC	STM1_A_RX_SERC	RX_AF	VDD3P3	VDD3P3	AP
18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	

Figure 5: PVG610X (XPIC) Pin Layout 18-34 (Top View)

2.2 PVG610A and PVG610X Common Signals Pin List

Ball Location	Ball Alias	Signal Name	Description	Reset State	Buffer Type	Dir.
J34	MDATA_0	INJCT_I_ADC_A_0	Injection bus I[11:0] and Q[11:0] input bus. External ADC A[11:0] and B[11:0] input busses External DAC I [11:0] and Q[11:0] output bus SDRAM Data[11:0] bidirection bus. SDRAM Address[11:0] output bus	I	LVCMOS I/O, 12ma	I
		DAC_I_0				O
		SDRAM_DATA_0				I/O
J33	MDATA_1	INJCT_I_ADC_A_1		I	LVCMOS I/O, 12ma	I
		DAC_I_1				O
		SDRAM_DATA_1				I/O
H34	MDATA_2	INJCT_I_ADC_A_2		I	LVCMOS I/O, 12ma	I
		DAC_I_2				O
		SDRAM_DATA_2				I/O
H32	MDATA_3	INJCT_I_ADC_A_3		I	LVCMOS I/O, 12ma	I
		DAC_I_3				O
		SDRAM_DATA_3				I/O
G32	MDATA_4	INJCT_I_ADC_A_4		I	LVCMOS I/O, 12ma	I
		DAC_I_4				O
		SDRAM_DATA_4				I/O
F34	MDATA_5	INJCT_I_ADC_A_5		I	LVCMOS I/O, 12ma	I
		DAC_I_5				O
		SDRAM_DATA_5				I/O
F32	MDATA_6	INJCT_I_ADC_A_6		I	LVCMOS I/O, 12ma	I
		DAC_I_6				O
		SDRAM_DATA_6				I/O
E32	MDATA_7	INJCT_I_ADC_A_7		I	LVCMOS I/O, 12ma	I
		DAC_I_7				O
		SDRAM_DATA_7				I/O
C33	MDATA_8	INJCT_I_ADC_A_8		I	LVCMOS I/O, 12ma	I
		DAC_I_8				O
		SDRAM_DATA_8				I/O
E33	MDATA_9	INJCT_I_ADC_A_9		I	LVCMOS I/O, 12ma	I
		DAC_I_9				O
		SDRAM_DATA_9				I/O
E34	MDATA_10	INJCT_I_ADC_A_10		I	LVCMOS I/O, 12ma	I
		DAC_I_10				O
		SDRAM_DATA_10				I/O
F31	MDATA_11	INJCT_I_ADC_A_11		I	LVCMOS I/O, 12ma	I
		DAC_I_11				O
		SDRAM_DATA_11				I/O
C30	MADDR_0	INJCT_Q_ADC_B_0		I	LVCMOS	I

Ball Location	Ball Alias	Signal Name	Description	Reset State	Buffer Type	Dir.
		DAC_Q_0			I/O, 12ma	O
		SDRAM_ADDROUT_0				O
D29	MADDR_1	INJCT_Q_ADC_B_1		I	LVCMOS	I
		DAC_Q_1			I/O, 12ma	O
		SDRAM_ADDROUT_1				O
A28	MADDR_2	INJCT_Q_ADC_B_2		I	LVCMOS	I
		DAC_Q_2			I/O, 12ma	O
		SDRAM_ADDROUT_2				O
B28	MADDR_3	INJCT_Q_ADC_B_3		I	LVCMOS	I
		DAC_Q_3			I/O, 12ma	O
		SDRAM_ADDROUT_3				O
C28	MADDR_4	INJCT_Q_ADC_B_4		I	LVCMOS	I
		DAC_Q_4			I/O, 12ma	O
		SDRAM_ADDROUT_4				O
C29	MADDR_5	INJCT_Q_ADC_B_5		I	LVCMOS	I
		DAC_Q_5			I/O, 12ma	O
		SDRAM_ADDROUT_5				O
A29	MADDR_6	INJCT_Q_ADC_B_6		I	LVCMOS	I
		DAC_Q_6			I/O, 12ma	O
		SDRAM_ADDROUT_6				O
B32	MADDR_7	INJCT_Q_ADC_B_7		I	LVCMOS	I
		DAC_Q_7			I/O, 12ma	O
		SDRAM_ADDROUT_7				O
A31	MADDR_8	INJCT_Q_ADC_B_8		I	LVCMOS	I
		DAC_Q_8			I/O, 12ma	
		SDRAM_ADDROUT_8				O
B30	MADDR_9	INJCT_Q_ADC_B_9		I	LVCMOS	I
		DAC_Q_9			I/O, 12ma	O
		SDRAM_ADDROUT_9				O
A30	MADDR_10	INJCT_Q_ADC_B_10		I	LVCMOS	I
		DAC_Q_10			I/O, 12ma	O
		SDRAM_ADDROUT_10				O
C32	MADDR_11	INJCT_Q_ADC_B_11		I	LVCMOS	I
		DAC_Q_11			I/O, 12ma	O
		SDRAM_ADDROUT_11				O
F30	MRASOUT	INJCT_CTRL_0	Injection bus control 0 input	I	LVCMOS	I
		SDRAM_N_RASOUT	sdram RAS control output		I/O, 12ma	O

Ball Location	Ball Alias	Signal Name	Description	Reset State	Buffer Type	Dir.
G30	MCASOUT	INJCT_STB_ADC_CLKIN	Injection bus input strobe External ADC input clock	I	LVCMOS I/O, 12ma	I
		SDRAM_N_CASOUT	sdram CAS control output			O
B31	MCLKOUT	INJCT_CTRL_3	Injection bus control 3 input	I	LVCMOS I/O, 24ma	I
		SDRAM_CLKOUT	sdram clock output			O
E30	MCSOUT	INJCT_CTRL_1	Injection bus control 1 input	I	LVCMOS I/O, 12ma	I
		SDRAM_N_DYCSOUT	sdram CS control output			O
H30	MWEOUT	INJCT_CTRL_2	Injection bus control 2 input	I	LVCMOS I/O, 12ma	I
		SDRAM_N_WEOUT	sdram WE control output			O
D34	MFBCLKIN	INJCT_CTRL_4	Injection bus control 4 input	I	LVCMOS I/O	I
		SDRAM_FBCLKIN	sdram feedback clock input			I
G33	MDATA_12	HOST_ADDR_1	Host Address[4:1] bidirectional bus Sdram Data [15:12] bidirectional bus	I	LVCMOS I/O, 12ma	I/O
		SDRAM_DATA_12				I/O
G34	MDATA_13	HOST_ADDR_2		I	LVCMOS I/O, 12ma	I/O
		SDRAM_DATA_13				I/O
H31	MDATA_14	HOST_ADDR_3		I	LVCMOS I/O, 12ma	I/O
		SDRAM_DATA_14				I/O
J32	MDATA_15	HOST_ADDR_4			LVCMOS I/O, 12ma	I/O
		SDRAM_DATA_15				I/O
J30	MDQMOUT_0	HOST_ADDR_5	Host Address[6:5] bidirectional bus Sdram DQM [1:0] output bus	I	LVCMOS I/O, 12ma	I/O
		SDRAM_DQMOUT_0				O
D30	MDQMOUT_1	HOST_ADDR_6		I	LVCMOS I/O, 12ma	I/O
		SDRAM_DQMOUT_1				O
E29	MADDR_12	HOST_ADDR_7	Host Address bus	I	LVCMOS I/O, 12ma	I/O
		SDRAM_ADDROUT_12	SDRAM parallel address bus			O
D32	MADDR_13	HOST_ADDR_8	Host Address bus	I	LVCMOS I/O, 12ma	I/O
		SDRAM_ADDROUT_13	SDRAM parallel address bus			O
D31	MADDR_14	HOST_ADDR_9	Host Address bus	I	LVCMOS I/O, 12ma	I/O
		SDRAM_ADDROUT_14	SDRAM parallel address bus			O
E22	ADC_CLK_N	ADC_CLK_N	AFE - ADC 10/12 clock input LVPECL negative.	I	LVPECL Input	I
E23	ADC_CLK_P	ADC_CLK_P	AFE - ADC 10/12 clock input LVPECL positive.	I	LVPECL Input	I
D20	IF_IN_P	IF_IN_P	AFE - ADC 10 bit - AC coupled Differential positive Input signal	I	Analog	I

Ball Location	Ball Alias	Signal Name	Description	Reset State	Buffer Type	Dir.
E20	IF_IN_N	IF_IN_N	AFE - ADC 10 bit - AC coupled Differential negative Input signal.	I	Analog	I
A25	BB_IN_I_P	BB_IN_I_P	AFE - ADC 12 bit channel 0 (I) - Differential positive Input signal.	I	Analog	I
A24	BB_IN_I_N	BB_IN_I_N	AFE - ADC 12 bit channel 0 (I) - Differential negeative Input signal.	I	Analog	I
B24	VCM_I	VCM_I	AFE – ADC Common Mode Voltage Output (I)	I	Analog	O
A20	BB_IN_Q_P	BB_IN_Q_P	AFE - ADC 12 bit channel 1 (Q) -Differential positive Input signal.		Analog	I
A21	BB_IN_Q_N	BB_IN_Q_N	AFE - ADC 12 bit channel 1 (Q) -Differential negeative Input signal.	I	Analog	I
B20	VCM_Q	VCM_Q	AFE – ADC Common Mode Voltage Output (Q)	I	Analog	O
E9	DAC_CLK_N	DAC_CLK_N	AFE - DAC clock input - LVPECL negative.	I	LVPECL Input	I
E10	DAC_CLK_P	DAC_CLK_P	AFE - DAC clock input - LVPECL positive.	I	LVPECL Input	I
A8	OUT_I_P	OUT_I_P	AFE - DAC channel 0 (I) Complementary Current Outputs	I	Analog	O
A9	OUT_I_N	OUT_I_N	AFE - DAC channel 0 (I) Complementary Current Outputs	I	Analog	O
A13	OUT_Q_P	OUT_Q_P	AFE - DAC channel 1 (Q) Complementary Current Outputs	I	Analog	O
A12	OUT_Q_N	OUT_Q_N	AFE - DAC channel 1 (Q) Complementary Current Outputs	I	Analog	O
B11	IREF	IREF	AFE - DAC Full-scale Current Reference for both Channels		Analog	
C27	RF_MUTE	RF_MUTE	Output signal for RF Mute in TDD mode. Asserted for all silence periods and deasserted for all transmission periods	I	LVCMOS I/O, 8ma	O
		BOOT_MODE_0	Boot mode 0 input			I
D26	TR_SWITCH	TR_SWITCH	Output signal to control an externa Tx/Rx switch in TDD mode. Asserted for all silence periods and deasserted for all transmission periods.	I	LVCMOS I/O, 8ma	O
		BOOT_MODE_1	Boot mode 1 input			I
E25	LNA_PD	LNA_PD	Output signal to control an externa LNA in TDD mode. Asserted for all transmission periods and deasserted for all silence periods.	I	LVCMOS I/O, 8ma	O
		BOOT_MODE_2	Boot mode 2 input			I

Ball Location	Ball Alias	Signal Name	Description	Reset State	Buffer Type	Dir.
A17	ENV_IN_P	ENV_IN_P	AFE - Envelope ADC - Differential positive Input signal.	I	Analog	I
A16	ENV_IN_N	ENV_IN_N	AFE - Envelope ADC - Differential negative Input signal.	I	Analog	I
B16	ENV_VCM	ENV_VCM	AFE – Envelope ADC - Common Mode Voltage Output	I	Analog	O
AC34	HOST_DATA_0	HOST_DATA_0	Host Data[15:0] bidirectional bus E1 External LIU RX LOS[15:0] input bus	I	LVCMOS I/O, 8ma	I/O
		RLOS_0				I
AA30	HOST_DATA_1	HOST_DATA_1		I	LVCMOS I/O, 8ma	I/O
		RLOS_1				I
Y34	HOST_DATA_2	HOST_DATA_2		I	LVCMOS I/O, 8ma	I/O
		RLOS_2				I
W34	HOST_DATA_3	HOST_DATA_3		I	LVCMOS I/O, 8ma	I/O
		RLOS_3				I
AB34	HOST_DATA_4	HOST_DATA_4		I	LVCMOS I/O, 8ma	I/O
		RLOS_4				I
V32	HOST_DATA_5	HOST_DATA_5		I	LVCMOS I/O, 8ma	I/O
		RLOS_5				I
V31	HOST_DATA_6	HOST_DATA_6		I	LVCMOS I/O, 8ma	I/O
		RLOS_6				I
V30	HOST_DATA_7	HOST_DATA_7		I	LVCMOS I/O, 8ma	I/O
		RLOS_7				I
AB31	HOST_DATA_8	HOST_DATA_8		I	LVCMOS I/O, 8ma	I/O
		RLOS_8				I
Y30	HOST_DATA_9	HOST_DATA_9		I	LVCMOS I/O, 8ma	I/O
		RLOS_9				I
Y32	HOST_DATA_10	HOST_DATA_10		I	LVCMOS I/O, 8ma	I/O
		RLOS_10				I
Y31	HOST_DATA_11	HOST_DATA_11		I	LVCMOS I/O, 8ma	I/O
		RLOS_11				I
AB30	HOST_DATA_12	HOST_DATA_12		I	LVCMOS I/O, 8ma	I/O
		RLOS_12				I
AB32	HOST_DATA_13	HOST_DATA_13		I	LVCMOS I/O, 8ma	I/O
		RLOS_13				
W33	HOST_DATA_14	HOST_DATA_14		I	LVCMOS I/O, 8ma	I/O
		RLOS_14				I
W30	HOST_DATA_15	HOST_DATA_15		I	LVCMOS I/O, 8ma	I/O
		RLOS_15				I
AA34	HOST_OE	HOST_OE	Host OE control, Bidirectional	I	LVCMOS I/O+ST, 8ma	I/O
		RLOS_16	E1 External LIU RX LOS[16] input			I

Ball Location	Ball Alias	Signal Name	Description	Reset State	Buffer Type	Dir.
AA33	HOST_WE	HOST_WE	Host WE control, Bidirectional	I	LVCMOS I/O+ST, 8ma	I/O
		RLOS_17	E1 External LIU RX LOS[17] input			I
AA32	HOST_ADDR_0	HOST_ADDR_0	Host Address 0, Bidirectional	I	LVCMOS I/O, 8ma	I/O
		RLOS_18	E1 External LIU RX LOS[18] input			I
V34	HOST_CS	HOST_CS	Host CS control, Bidirectional	I	LVCMOS I/O+ST, 8ma	I/O
		RLOS_19	E1 External LIU RX LOS[19] input			I
AC32	HOST_DPRAM_IRQ	HOST_DPRAM_IRQ	Low level interrupt signal (for the parallel bus). Active Low. Output when using internal DPRAM and vice versa.	I	LVCMOS I/O Open drain + PU, 8ma	I/O
		RLOS_20	E1 RX LOS 20			I
AC33	HOST_INT	HOST_INT	Main Interrupt Output. Active Low.	O	LVCMOS I/O Open drain + PU, 8ma	O
W32	XPIC_HOST_CS_N	XPIC_HOST_CS_N	Chip Select for XPIC chip	O	LVCMOS I/O, 8ma	O
K30	TEST_0	TEST_0	Test bus [30:0]	I	LVCMOS I/O, 8ma	O
K31	TEST_1	TEST_1				O
L30	TEST_2	TEST_2				O
L32	TEST_3	TEST_3				O
M30	TEST_4	TEST_4				O
M31	TEST_5	TEST_5				O
N30	TEST_6	TEST_6				O
N32	TEST_7	TEST_7				O
P30	TEST_8	TEST_8				O
P31	TEST_9	TEST_9				O
R30	TEST_10	TEST_10				O
R32	TEST_11	TEST_11				O
T30	TEST_12	TEST_12				O
T31	TEST_13	TEST_13				O
U30	TEST_14	TEST_14				O
U32	TEST_15	TEST_15				O
K32	TEST_16	TEST_16				O
K34	TEST_17	TEST_17				O
L33	TEST_18	TEST_18				O
L34	TEST_19	TEST_19				O
M32	TEST_20	TEST_20				O
M34	TEST_21	TEST_21				O
N33	TEST_22	TEST_22				O

Ball Location	Ball Alias	Signal Name	Description	Reset State	Buffer Type	Dir.
N34	TEST_23	TEST_23				O
P32	TEST_24	TEST_24				O
P34	TEST_25	TEST_25				O
R33	TEST_26	TEST_26				O
R34	TEST_27	TEST_27				O
T32	TEST_28	TEST_28				O
T34	TEST_29	TEST_29				O
U33	TEST_30	TEST_30				O
U34	TEST_31	TEST_31	Test bus [31]	I	LVCMOS I/O, 12ma	O
AP5	JTAG_TCK	JTAG_TCK	JTAG Test Clock	I	LVCMOS Input	I
AN3	JTAG_TDI	JTAG_TDI	JTAG Test Data Input	I	LVCMOS Input+ PU	I
AP6	JTAG_TDO	JTAG_TDO	JTAG Test Data Output	O	LVCMOS Output, 8ma	O
AP4	JTAG_TMS	JTAG_TMS	JTAG Test Mode Select	I	LVCMOS Input+ PU	I
AN4	JTAG_TRST	JTAG_TRST	JTAG Reset	I	LVCMOS Input+ ST+PU	I
AN5	JTAG_SEL	JTAG_SEL	JTAG Selector: 0 - Normal Jtag Interface 1 - Used when Jtag pins are connected to an external MultiICE debug hardware to debug ARM Core	I	LVCMOS Input+ ST+PD	I
A3	SYS_CLK_N	SYS_CLK_N	Input Reference core chip clock negative.		LVPECL Input	I
A4	SYS_CLK_P	SYS_CLK_P	Input Reference core chip clock positive.		LVPECL Input	I
D27	SPI_M2_CS_0	SPI_M2_CS_0	Primary SPI Master interface DC Correction interface	O	LVCMOS I/O, 8ma	O
		DC_COR_I				O
E27	SPI_M2_DO	SPI_M2_DO		O	LVCMOS I/O, 8ma	O
		DC_COR_Q				O
D28	SPI_M2_DI	SPI_M2_DI		I	LVCMOS I/O, 8ma	I
		DC_COR_EN				O
E28	SPI_M2_CLK	SPI_M2_CLK		O	LVCMOS I/O, 12ma	O
		DC_COR_CLK				O
E26	AGC_PWM	AGC_PWM	This signal feeds an external filter, which creates an analog voltage for an external AGC	I	LVCMOS I/O, 8ma	O
		BOOT_MODE_3	Boot mode 3 input			I

Ball Location	Ball Alias	Signal Name	Description	Reset State	Buffer Type	Dir.
AP22	NRESET	NRESET	Hardware Reset. Active low.	I	LVCMOS Input+ ST+PU	I
AP23	CPU_NRESET	CPU_NRESET	CPU Reset. Active low.	I	LVCMOS Input+ ST+PU	I
AP21	NRESET_OUT	RESET_OUT_N	Internal chip reset indication. When hardware reset is asserted. The signal is deasserted 256 system clock cycles (clock before PVG610A PLL), after the PVG610A NRESET input is deasserted This pin is open drain.	O	LVCMOS I/O+ open drain+ PU, 8ma	O
AN22	AIRLOSS	ALARM_AIRLOSS	Modem Air Loss alarm condition.	O	LVCMOS I/O, 8ma	O
AM28	SYS_CLK_OUT	SYS_CLK_OUT	Outputs SYS_CLK or SYS_CLK/2 (can also be disabled, remain idle). Maximum frequency is 100MHz	O	LVCMOS I/O, 12ma	O
		PLL_L	PLL lock indicator			O
AL21	WD	WD	WatchDog timer expired inidication. or patting signal for external WD device	O	LVCMOS I/O, 8ma	O
		RTCK	Adaptive JTAG clock for MultiICE.			O
AM27	TXP_IN_DATA_0	TXP_IN_DATA_0	Protection TX Data[7:0] bus Input Protection TX Data[7:0] bus Output	I	LVCMOS I/O, 8ma	I
		TXP_OUT_DATA_0				O
AM25	TXP_IN_DATA_1	TXP_IN_DATA_1		I	LVCMOS I/O, 8ma	I
		TXP_OUT_DATA_1				O
AM23	TXP_IN_DATA_2	TXP_IN_DATA_2		I	LVCMOS I/O, 8ma	I
		TXP_OUT_DATA_2				O
AM22	TXP_IN_DATA_3	TXP_IN_DATA_3		I	LVCMOS I/O, 8ma	I
		TXP_OUT_DATA_3				O
AN26	TXP_IN_DATA_4	TXP_IN_DATA_4		I	LVCMOS I/O, 8ma	I
		TXP_OUT_DATA_4				O
AN24	TXP_IN_DATA_5	TXP_IN_DATA_5		I	LVCMOS I/O, 8ma	I
		TXP_OUT_DATA_5				O
AP25	TXP_IN_DATA_6	TXP_IN_DATA_6		I	LVCMOS I/O, 8ma	I
		TXP_OUT_DATA_6				O
AP24	TXP_IN_DATA_7	TXP_IN_DATA_7		I	LVCMOS I/O, 8ma	I
		TXP_OUT_DATA_7				O
AP26	TXP_IN_STB	TXP_IN_STB	Protection TX Strobe Input	I	LVCMOS I/O, 8ma	I
		TXP_OUT_STB	Protection TX Strobe Output			O
AP27	TXP_IN_SYNC	TXP_IN_SYNC	Protection TX Sync Input	I	LVCMOS I/O, 8ma	I
		TXP_OUT_SYNC	Protection TX Sync Output			O

Ball Location	Ball Alias	Signal Name	Description	Reset State	Buffer Type	Dir.
AK27	RXP_IN_DATA_0	RXP_IN_DATA_0	Protection RX Data[7:0] bus Input Protection RX Data[7:0] bus Output	I	LVCMOS I/O, 8ma	I
		RXP_OUT_DATA_0				O
AK26	RXP_IN_DATA_1	RXP_IN_DATA_1		I	LVCMOS I/O, 8ma	I
		RXP_OUT_DATA_1				O
AK23	RXP_IN_DATA_2	RXP_IN_DATA_2		I	LVCMOS I/O, 8ma	I/O
		RXP_OUT_DATA_2				O
AK22	RXP_IN_DATA_3	RXP_IN_DATA_3		I	LVCMOS I/O, 8ma	I
		RXP_OUT_DATA_3				O
AL27	RXP_IN_DATA_4	RXP_IN_DATA_4		I	LVCMOS I/O, 8ma	I
		RXP_OUT_DATA_4				O
AL25	RXP_IN_DATA_5	RXP_IN_DATA_5		I	LVCMOS I/O, 8ma	I
		RXP_OUT_DATA_5				O
AL23	RXP_IN_DATA_6	RXP_IN_DATA_6		I	LVCMOS I/O, 8ma	I
		RXP_OUT_DATA_6				O
AM26	RXP_IN_DATA_7	RXP_IN_DATA_7		I	LVCMOS I/O, 8ma	I
		RXP_OUT_DATA_7				O
AK24	RXP_IN_STB	RXP_IN_STB	Protection RX Strobe Input	I	LVCMOS I/O, 8ma	I
		RXP_OUT_STB	Protection RX Strobe Output			O
AK25	RXP_IN_SYNC	RXP_IN_SYNC	Protection RX Sync Input	I	LVCMOS I/O, 8ma	I
		RXP_OUT_SYNC	Protection RX Sync Output			O
AM24	RXP_IN_UC	RXP_IN_UC	Protection RX UnCorr Input	I	LVCMOS I/O, 8ma	I
		RXP_OUT_UC	Protection RX UnCorr Output			O
AN32	STM1_REF_CLK	STM1_REF_CLK	19.44MHz input reference clock	I	LVCMOS I/O, 8ma	I
AK28	DDS3	DDS3	Direct Digital Synthesis 3	I	LVCMOS I/O, 8ma	O
AL29	DDS4	DDS4	Direct Digital Synthesis 4	I	LVCMOS I/O, 8ma	O
AM33	STM1_A_RX_FP	STM1_A_RX_FP	TOH (line A) Rx Frame pulse	I	LVCMOS I/O, 8ma	O
		DDS5	Direct Digital Synthesis 5	I		O
AH34	STM1_A_RX_CLK	STM1_A_RX_CLK	STM1-A Receive Parallel Input Clock at 19.44 MHz	I	LVCMOS I/O, 8ma	I
AK29	STM1_A_RX_LOSS	STM1_A_RX_LOSS	STM1-A Loss of Signal	I	LVCMOS I/O, 8ma	I
AL32	RX_DATA_0	RX_DATA_0	GPI RX Data[7:0] Output bus. STM1_A TX Data[7:0] Output bus	I	LVCMOS I/O, 8ma	O
		STM1_A_TX_DATA_0				O
AL34	RX_DATA_1	RX_DATA_1		I	LVCMOS I/O, 8ma	O
		STM1_A_TX_DATA_1				O
AK32	RX_DATA_2	RX_DATA_2		I	LVCMOS I/O, 8ma	O
		STM1_A_TX_DATA_2				O
AK31	RX_DATA_3	RX_DATA_3		I	LVCMOS I/O, 8ma	O
		STM1_A_TX_DATA_3				O

Ball Location	Ball Alias	Signal Name	Description	Reset State	Buffer Type	Dir.
AJ34	RX_DATA_4	RX_DATA_4		I	LVCMOS I/O, 8ma	O
		STM1_A_TX_DATA_4				O
AJ32	RX_DATA_5	RX_DATA_5		I	LVCMOS I/O, 8ma	O
		STM1_A_TX_DATA_5				O
AJ33	RX_DATA_6	RX_DATA_6		I	LVCMOS I/O, 8ma	O
		STM1_A_TX_DATA_6				O
AH31	RX_DATA_7	RX_DATA_7		I	LVCMOS I/O, 8ma	O
		STM1_A_TX_DATA_7				O
AF31	TX_DATA_0	TX_DATA_0	GPI TX Data[7:0] Input bus. STM1_A RX Data[7:0] Input bus	I	LVCMOS I/O	I
		STM1_A_RX_DATA_0				I
AF32	TX_DATA_1	TX_DATA_1		I	LVCMOS I/O	I
		STM1_A_RX_DATA_1				I
AE34	TX_DATA_2	TX_DATA_2		I	LVCMOS I/O	I
		STM1_A_RX_DATA_2				I
AE32	TX_DATA_3	TX_DATA_3		I	LVCMOS I/O	I
		STM1_A_RX_DATA_3				I
AE33	TX_DATA_4	TX_DATA_4		I	LVCMOS I/O	I
		STM1_A_RX_DATA_4				I
AD34	TX_DATA_5	TX_DATA_5		I	LVCMOS I/O	I
		STM1_A_RX_DATA_5				I
AD31	TX_DATA_6	TX_DATA_6		I	LVCMOS I/O	I
		STM1_A_RX_DATA_6				I
AD32	TX_DATA_7	TX_DATA_7		I	LVCMOS I/O	I
		STM1_A_RX_DATA_7				I
AE30	TX_AF	TX_AF	GPI TX Fifo Almost Full output	I	LVCMOS I/O, 8ma	O
AF34	TX_AE	TX_AE	GPI TX Fifo Almost Empty output	I	LVCMOS I/O, 8ma	O
		STM1_A_TX_CLK	STM1-A Transmit Parallel output Clock at 19.44 MHz.			O
AF30	TX_WE	TX_WE	GPI TX Write Enable.Input	I	LVCMOS I/O	I
AG34	TX_CLK	TX_CLK	GPI TX Clock Input	I	LVCMOS I/O	I
AH32	RX_CLK	RX_CLK	GPI RX Clock Input	I	LVCMOS I/O	I
AC30	TX_SYNC	TX_SYNC	GPI TX Sync - Bidirectional – Sync signal	I	LVCMOS I/O, 8ma	I/O
AD30	TX_ACM	TX_ACM	GPI TX ACM 4 bit serial data - indicates the ACM profile of the next Airframe	I	LVCMOS I/O, 8ma	O
AJ30	RX_SYNC	RX_SYNC	GPI RX Sync- Output Sync signal	I	LVCMOS I/O, 8ma	O

Ball Location	Ball Alias	Signal Name	Description	Reset State	Buffer Type	Dir.
AP32	RX_AF	RX_AF	GPI RX Fifo Almost Full output	I	LVCMOS I/O, 8ma	O
AG30	RX_AE	RX_AE	GPI RX Fifo Almost Empty output	I	LVCMOS I/O, 8ma	O
AH30	RX_RE	RX_RE	GPI RX Read Enable input	I	LVCMOS I/O, 8ma	I
AG32	RX_ACM	RX_ACM	GPI RX ACM 4 bit serial data - indicates the ACM profile of the current Airframe.	I	LVCMOS I/O, 8ma	O
AG33	RX_UNCOR	RX_UNCOR	GPI RX Uncorr output	I	LVCMOS I/O, 8ma	O
AN31	STM1_A_RX_D_OUT	STM1_A_RX_DATA_OUT	TOH (line A) RX data output.	I	LVCMOS I/O, 8ma	O
		DDS0	Direct Digital Synthesis			O
AP31	STM1_A_RX_SER_C	STM1_A_RX_SER_CLK	TOH (line A) RX clock	I	LVCMOS I/O, 8ma	O
		DDS1	Direct Digital Synthesis			O
AM29	STM1_A_TX_D_OUT	STM1_A_TX_DATA_OUT	TOH (line A) TX Data output.	I	LVCMOS I/O, 8ma	O
		DDS2	Direct Digital Synthesis			O
AP30	STM1_A_TX_SER_C	STM1_A_TX_SER_CLK	TOH (line A) TX clock	I	LVCMOS I/O, 8ma	O
		DDS6	Direct Digital Synthesis			O
AL30	STM1_A_TX_FP	STM1_A_TX_FP	TOH (line A) Tx Frame pulse.	I	LVCMOS I/O, 8ma	O
		DDS7	Direct Digital Synthesis			O
AM30	STM1_A_TX_D_IN	STM1_A_TX_DATA_IN	TOH (Line A) Tx Data Input	I	LVCMOS I/O	I
		DDS_CLK	Direct Digital Synthesis clock			I
AL33	STM1_A_VCXO_PWM	STM1_A_VCXO_PWM	STM1-A Pulse Width Modulated signal. The PWM stream has 8-bit resolution to provide 256 discrete output levels. The stream should be externally low-pass filtered to create a smooth voltage control for VCXO	I	LVCMOS I/O, 8ma	O
AM31	STM1_A_RX_D_IN	STM1_A_RX_DATA_IN	TOH (Line A) Rx Data Input	I	LVCMOS I/O	I
AK34	STM1_A_VCXO_CLK	STM1_A_VCXO_CLK	STM1-A Transmit VCXO Input Clock. This is a 19.44MHz clock, which is the output of the VCXO.	I	LVCMOS I/O	I
AP14	MII_TX_CLK	MII_TX_CLK	MII Tx clock (2.5MHz or 25Mhz for MII, 125MHz for GMII)	I	LVCMOS I/O	I
		INJCT2_I_ADC2_A_8	Secondary Injection bus I[8] input Secondary External ADC A[8] input			I
AP11	MII_TX_EN	MII_TX_EN	MII Tx Enable - valid data is present	I	LVCMOS I/O,	O

Ball Location	Ball Alias	Signal Name	Description	Reset State	Buffer Type	Dir.
		STM1_B_TX_CLK	STM1-B Transmit Parallel output Clock at 19.44 MHz		12ma	O
		INJCT2_I_ADC2_A_9	Secondary Injection bus I[9] input Secondary External ADC A[9] input			I
AL10	MII_TX_ER	MII_TX_ER	MII TX error indication	I	LVCMOS I/O, 12ma	O
		STM1_B_VCXO_PWM	STM1B PWM output. This pad is connected to the STM1B VCXO			O
		INJCT2_I_ADC2_A_10	Secondary Injection bus I[10] input Secondary External ADC A[10] input			I
AN13	MII_TXD_0	MII_TXD_0	GMII TX Data[7:0] output (for MII use only TXD [3:0]). STM1B TX Data[7:0] output Secondary Injection bus I[7:0] input Secondary External ADC A[7:0] input	I	LVCMOS I/O, 12ma	O
		STM1_B_TX_DATA_0				O
		INJCT2_I_ADC2_A_0				I
AM13	MII_TXD_1	MII_TXD_1		I	LVCMOS I/O, 12ma	O
		STM1_B_TX_DATA_1				O
		INJCT2_I_ADC2_A_1				I
AP13	MII_TXD_2	MII_TXD_2		I	LVCMOS I/O, 12ma	O
		STM1_B_TX_DATA_2				O
		INJCT2_I_ADC2_A_2				I
AM12	MII_TXD_3	MII_TXD_3		I	LVCMOS I/O, 12ma	O
		STM1_B_TX_DATA_3				O
		INJCT2_I_ADC2_A_3				I
AL12	MII_TXD_4	MII_TXD_4		I	LVCMOS I/O, 12ma	O
		STM1_B_TX_DATA_4				O
		INJCT2_I_ADC2_A_4				I
AP12	MII_TXD_5	MII_TXD_5		I	LVCMOS I/O, 12ma	O
		STM1_B_TX_DATA_5				O
		INJCT2_I_ADC2_A_5				I
AN11	MII_TXD_6	MII_TXD_6		I	LVCMOS I/O, 12ma	O
		STM1_B_TX_DATA_6				O
		INJCT2_I_ADC2_A_6				I
AM11	MII_TXD_7	MII_TXD_7		I	LVCMOS I/O, 12ma	O
		STM1_B_TX_DATA_7				O
		INJCT2_I_ADC2_A_7				I
AP7	MII_RXD_0	MII_RXD_0	GMII RX Data[7:0] Input (for MII use only TXD [3:0]) STM1B RX Data[7:0] input Secondary Injection bus Q[7:0] input Secondary External ADC B[7:0] input	I	LVCMOS I/O	I
		STM1_B_RX_DATA_0				I
		INJCT2_Q_ADC2_B_0				I
AM7	MII_RXD_1	MII_RXD_1		I	LVCMOS I/O	I
		STM1_B_RX_DATA_1				I

Ball Location	Ball Alias	Signal Name	Description	Reset State	Buffer Type	Dir.
		INJCT2_Q_ADC2_B_1				I
AN7	MII_RXD_2	MII_RXD_2		I	LVCMOS I/O	I
		STM1_B_RX_DATA_2				I
		INJCT2_Q_ADC2_B_2				I
AP8	MII_RXD_3	MII_RXD_3		I	LVCMOS I/O	I
		STM1_B_RX_DATA_3				I
		INJCT2_Q_ADC2_B_3				I
AL8	MII_RXD_4	MII_RXD_4		I	LVCMOS I/O	I
		STM1_B_RX_DATA_4				I
		INJCT2_Q_ADC2_B_4				I
AM8	MII_RXD_5	MII_RXD_5		I	LVCMOS I/O	I
		STM1_B_RX_DATA_5				I
		INJCT2_Q_ADC2_B_5				I
AP9	MII_RXD_6	MII_RXD_6		I	LVCMOS I/O	I
		STM1_B_RX_DATA_6				I
		INJCT2_Q_ADC2_B_6				I
AM9	MII_RXD_7	MII_RXD_7		I	LVCMOS I/O	I
		STM1_B_RX_DATA_7				I
		INJCT2_Q_ADC2_B_7				I
AN9	MII_RX_DV	MII_RX_DV	MII RX Data Valid	I	LVCMOS I/O	I
		STM1_B_RX_CLK	Receive Parallel Input Clock at 19.44 MHz			I
		INJCT2_STB_ADC2_CLKIN	Secondary Injection bus Strobe input Secondary External ADC clock input			I
AP10	MII_RX_ER	MII_RX_ER	MII RX Error	I	LVCMOS I/O	I
		STM1_B_RX_LOSS	STM1-B Loss of Signal.			I
AM10	MII_RX_CLK	MII_RX_CLK	Rx clock (2.5MHz or 25MHz for MII, 125MHz for GMII).	I	LVCMOS I/O	I
		STM1_B_VCXO_CLK	STM1-B Transmit VCXO Input Clock. This is a 19.44MHz clock, which is the output of the VCXO			I
AK8	MII_COL	MII_COL	Collision Detected - Indicates collision detected. This input remains High for the duration of the collision. This signal is asynchronous and is inactive during full-duplex operation	I	LVCMOS I/O	I
		INJCT2_I_ADC2_A_11	Secondary Injection bus I[11] input Secondary External ADC A[11] input			I

Ball Location	Ball Alias	Signal Name	Description	Reset State	Buffer Type	Dir.
AK7	MII_CRS	MII_CRS	CARRIER SENSE - Asserted high to indicate the presence of carrier due to receive or transmit activity in 10BASE-T or 100BASETX Half Duplex Modes, while in full duplex mode carrier sense is asserted to indicate the presence of carrier due only to receive activity.	I	LVCMOS I/O	I
		INJCT2_CTRL_4	Secondary Injection ctrl[4] input			I
AL6	MII_MDIO	MII_MDIO	Management Data I/O - Data input/output for the IEEE 802.3u compliant Management and Status interface	I	LVCMOS I/O, 8ma	I/O
		STM1_B_RX_FP	TOH (line B) RX Frame pulse			O
		INJCT2_CTRL_0	Secondary Injection ctrl[0] input			I
AM6	MII_MDC	MII_MDC	Management Data clock - Synchronous clock to the MDIO management data input/output serial interface, which may be asynchronous to transmit and receive clocks. The maximum clock rate is 25 MHz with no minimum clock rate.	I	LVCMOS I/O, 8ma	O
		STM1_B_RX_SER_CLK	TOH (line B) RX clock output			O
		INJCT2_Q_ADC2_B_8	Secondary Injection bus Q[8] input Secondary External ADC B[8] input			I
AK10	MII_TBI_62_RX_C	INJCT2_Q_ADC2_B_9	Secondary Injection bus Q[9] input Secondary External ADC B[9] input	I	LVCMOS I/O	I
AK14	STM1_B_TX_D_IN	STM1_B_TX_DATA_IN	TOH (line B) TX data input	I	LVCMOS I/O	I
		INJCT2_Q_ADC2_B_10	Secondary Injection bus Q[10] input Secondary External ADC B[10] input			I
AK13	STM1_B_TX_FP	STM1_B_TX_FP	TOH (line B) TX Frame pulse	I	LVCMOS I/O, 8ma	O
		INJCT2_Q_ADC2_B_11	Secondary Injection bus Q[11] input Secondary External ADC B[11] input			I
AK12	STM1_B_TX_SER_C	STM1_B_TX_SER_CLK	TOH (line B) TX clock output	I	LVCMOS I/O, 8ma	O
		INJCT2_CTRL_3	Secondary Injection ctrl[3] input			I
AL14	HOST_ADDR_10	HOST_ADDR_10	Host Address bus	I	LVCMOS I/O, 8ma	I/O
		INJCT2_CTRL_1	Secondary Injection ctrl[1] input			I
AM14	HOST_ADDR_11	HOST_ADDR_11	Host Address bus	I	LVCMOS I/O, 8ma	I/O
		INJCT2_CTRL_2	Secondary Injection ctrl[2] input			I

Ball Location	Ball Alias	Signal Name	Description	Reset State	Buffer Type	Dir.
AK15	STM1_B_TX_D_OUT	STM1_B_TX_DATA_OUT	TOH (line B) TX data output	I	LVCMOS I/O, 8ma	O
AK9	STM1_B_RX_D_IN	STM1_B_RX_DATA_IN	TOH (line B) RX data input	I	LVCMOS I/O	I
AK11	STM1_B_RX_D_OUT	STM1_B_RX_DATA_OUT	TOH (line B) RX data output	I	LVCMOS I/O, 8ma	O
AP28	EOW_CLK	EOW_CLK	Transmit Clock, clock output for the PCM data, the frequency is 64KHz or 128KHz	I	LVCMOS I/O, 8ma	O
AN28	EOW_FP	EOW_FP	EOW Frame pulse. PCM data 8 kHz synchronous signal output.	I	LVCMOS I/O, 8ma	O
AP29	EOW_TDATA	EOW_TDATA	Transmit PCM data output.	I	LVCMOS I/O, 8ma	O
AN29	EOW_RDATA	EOW_RDATA	Receive PCM data input.	I	LVCMOS I/O	I
AP15	OMI_TCLK	OMI_TCLK	OMI Transmit Clock. Up to 10MHz	I	LVCMOS I/O, 8ma	O
		HDLC_TCLK	Input Transmit HDLC Clock , up to 10 MHz			I
AN15	OMI_TXD	OMI_TXD	OMI Transmitted serial data	I	LVCMOS I/O, 8ma	I
		HDLC_TXD	Output transmit serial HDLC data	I		O
AP16	OMI_RCLK	OMI_RCLK	OMI receive clock upto 10 MHz	I	LVCMOS I/O, 8ma	O
		HDLC_RCLK	Input receive HDLC clock up to 10 MHz	I		I
AN16	OMI_RXD	OMI_RXD	OMI receive serial data	I	LVCMOS I/O, 8ma	O
		HDLC_RXD	Input receive serial HDLC data	I		I
AP19	UART_RXD	UART_RXD	UART Receive Serial data input	I	LVCMOS I/O	I
AP20	UART_TXD	UART_TXD	UART Transmit Serial data output	O	LVCMOS I/O, 8ma	O
AM17	SPI_M_CS_0	SPI_M_CS_0	SPI Master chip select[0] output	I	LVCMOS I/O, 8ma	O
		SPI_S_CS	SPI Slave chip select input.			I
AP17	SPI_M_CLK	SPI_M_CLK	SPI master clock output	I	LVCMOS I/O, 12ma	O
		SPI_S_CLK	SPI slave clock input			I
AN17	SPI_M_DI	SPI_M_DI	SPI master data input	I	LVCMOS I/O	I
		SPI_S_DI	SPI slave data input			I
AP18	SPI_M_DO	SPI_M_DO	SPI master data output	I	LVCMOS I/O, 8ma	O
		SPI_S_DO	SPI slave data output			O
AM15	I2C_SCL	I2C_SCL	I2C Serial clock input/output	I	LVCMOS I/O+open drain, 8ma	I/O

Ball Location	Ball Alias	Signal Name	Description	Reset State	Buffer Type	Dir.
AM16	I2C_SDA	I2C_SDA	I2C Serial data	I	LVCMOS I/O+ open drain, 8ma	I/O
AK16	GPIO_0	GPIO_0	General Purpose [0] Input/Output signal. Driven or read by the CPU.	I	LVCMOS I/O, 8ma	I/O
		DFT_0	testmode[0] selector input. Used only when DFT_TEST pin is hight	I		I
AK17	GPIO_1	GPIO_1	General Purpose [1] Input/Output signal. Driven or read by the CPU.	I	LVCMOS I/O, 8ma	I/O
		DFT_1	testmode[1] selector input. Used only when DFT_TEST pin is hight	I		I
AK18	GPIO_2	GPIO_2	General Purpose [2] Input/Output signal. Driven or read by the CPU.	I	LVCMOS I/O, 8ma	I/O
		DFT_2	testmode[2] selector input. Used only when DFT_TEST pin is hight	I		I
AK19	GPIO_3	GPIO_3	General Purpose [3] Input/Output signal. Driven or read by the CPU.	I	LVCMOS I/O, 8ma	I/O
AM19	GPIO_4	GPIO_4	General Purpose [4] Input/Output signal. Driven or read by the CPU.	I	LVCMOS I/O, 8ma	I/O
		HOST_ADDR_12	Host Address[12] bidirectional bus	I		I/O
		SPI_M_CS_4	SPI Master chip select[4] output	I		O
AM20	GPIO_5	GPIO_5	General Purpose [5] Input/Output signal. Driven or read by the CPU.	I	LVCMOS I/O, 8ma	I/O
		HOST_ADDR_13	Host Address[13] bidirectional bus	I		I/O
		SPI_M_CS_5	SPI Master chip select[5] output	I		O
AN19	GPIO_6	GPIO_6	General Purpose [6] Input/Output signal. Driven or read by the CPU.	I	LVCMOS I/O, 8ma	I/O
		HOST_ADDR_14	Host Address[14] bidirectional bus	I		I/O
		SPI_M_CS_6	SPI Master chip select[6] output	I		O
AN20	GPIO_7	GPIO_7	General Purpose [7] Input/Output signal. Driven or read by the CPU.	I	LVCMOS I/O, 8ma	I/O
		HOST_ADDR_15	Host Address[15] bidirectional bus	I		I/O
		SPI_M_CS_7	SPI Master chip select[6] output	I		O

Ball Location	Ball Alias	Signal Name	Description	Reset State	Buffer Type	Dir.
AK20	GPIO_8	GPIO_8	General Purpose [8] Input/Output signal. Driven or read by the CPU.	I	LVCMOS I/O, 8ma	I/O
		EVENT_PHY_IRQ	PHY Alarm event for debug	I		O
AL16	GPIO_9	GPIO_9	General Purpose [9] Input/Output signal. Driven or read by the CPU.	I	LVCMOS I/O, 8ma	I/O
		ALARM_RX_NET_IRQ	Alarm RX interrupt. For debug	I		O
AM21	GPIO_10	GPIO_10	General Purpose [10] Input/Output signal. Driven or read by the CPU.	I	LVCMOS I/O, 12ma	I/O
		TXP_CLKOUT	This is a clock signal running at half the SYS_CLK frequency. Can be used as input clock to protection bus SERDES.	I		O
AL17	GPIO_11	GPIO_11	General Purpose [11] Input/Output signal. Driven or read by the CPU.	I	LVCMOS I/O, 8ma	I/O
		ALARM_TX_NET_IRQ	Alarm TX interrupt. For debug purposes.	I		O
AK21	GPIO_12	GPIO_12	General Purpose [12] Input/Output signal. Driven or read by the CPU.	I	LVCMOS I/O, 12ma	I/O
		RXP_CLKOUT	This is a clock signal running at half the SYS_CLK frequency. Can be used as input clock to protection bus SERDES.	I		O
AL18	GPIO_13	GPIO_13	General Purpose [13] Input/Output signal. Driven or read by the CPU.	I	LVCMOS I/O, 8ma	I/O
		SPI_M_CS_1	SPI Master chip select[1] output	I		O
AL20	GPIO_14	GPIO_14	General Purpose [14] Input/Output signal. Driven or read by the CPU.	I	LVCMOS I/O, 8ma	I/O
		SPI_M_CS_2	SPI Master chip select[2] output	I		O
AM18	GPIO_15	GPIO_15	General Purpose [15] Input/Output signal. Driven or read by the CPU.	I	LVCMOS I/O, 8ma	I/O
		SPI_M_CS_3	SPI Master chip select[3] output	I		O
AM5	DFT_TEST	DFT_TEST	Test mode control. When high, one of 8 test modes are activated. The test nodes are selected by DFT[2:0]	I	LVCMOS Input+ PD	I
A6	SPARE_0	SPARE_0	ADC Single ended clock input	I	LVCMOS Input	I
B6	SPARE_1	SPARE_1	System Single ended reference clock input	I	LVCMOS Input	I
C6	SPARE_2	SPARE_2	DAC Single ended clock input	I	LVCMOS Input	I

Notes:

1. The electrical current figures in the Buffer Type column represent the drive power
2. I/O's with ST indication have internal Schmitt Trigger circuit.
3. I/O's with PU indication have internal Pull-up resistor
4. I/O's with PD indication have internal Pull-down resistor

2.3 PVG610A Exclusive, Signals Pin List

Ball Location	Ball Alias	Signal Name	Description	Reset State	Type	Dir.
AK4	RTIP_0	RPOS_0	Receive E1/T1/J1 serial data	I	LVCMOS	I
		RTIP_0	Receive Bipolar E1/T1/J1 Tip		Analog	I
AJ4	RTIP_1	RPOS_1	Receive E1/T1/J1 serial data	I	LVCMOS	I
		RTIP_1	Receive Bipolar E1/T1/J1 Tip		Analog	I
AH4	RTIP_2	RPOS_2	Receive E1/T1/J1 serial data	I	LVCMOS	I
		RTIP_2	Receive Bipolar E1/T1/J1 Tip		Analog	I
AF4	RTIP_3	RPOS_3	Receive E1/T1/J1 serial data	I	LVCMOS	I
		RTIP_3	Receive Bipolar E1/T1/J1 Tip		Analog	I
AE4	RTIP_4	RPOS_4	Receive E1/T1/J1 serial data	I	LVCMOS	I
		RTIP_4	Receive Bipolar E1/T1/J1 Tip		Analog	I
AD4	RTIP_5	RPOS_5	Receive E1/T1/J1 serial data	I	LVCMOS	I
		RTIP_5	Receive Bipolar E1/T1/J1 Tip		Analog	I
AB4	RTIP_6	RPOS_6	Receive E1/T1/J1 serial data	I	LVCMOS	I
		RTIP_6	Receive Bipolar E1/T1/J1 Tip		Analog	I
AA4	RTIP_7	RPOS_7	Receive E1/T1/J1 serial data	I	LVCMOS	I
		RTIP_7	Receive Bipolar E1/T1/J1 Tip		Analog	I
Y4	RTIP_8	RPOS_8	Receive E1/T1/J1 serial data	I	LVCMOS	I
		RTIP_8	Receive Bipolar E1/T1/J1 Tip		Analog	I
V2	RTIP_9	RPOS_9	Receive E1/T1/J1 serial data	I	LVCMOS	I
		RTIP_9	Receive Bipolar E1/T1/J1 Tip		Analog	I
U2	RTIP_10	RPOS_10	Receive E1/T1/J1 serial data	I	LVCMOS	I
		RTIP_10	Receive Bipolar E1/T1/J1 Tip		Analog	I
T2	RTIP_11	RPOS_11	Receive E1/T1/J1 serial data	I	LVCMOS	I
		RTIP_11	Receive Bipolar E1/T1/J1 Tip		Analog	I
P2	RTIP_12	RPOS_12	Receive E1/T1/J1 serial data	I	LVCMOS	I
		RTIP_12	Receive Bipolar E1/T1/J1 Tip		Analog	I
N2	RTIP_13	RPOS_13	Receive E1/T1/J1 serial data	I	LVCMOS	I
		RTIP_13	Receive Bipolar E1/T1/J1 Tip		Analog	I
M2	RTIP_14	RPOS_14	Receive E1/T1/J1 serial data	I	LVCMOS	I
		RTIP_14	Receive Bipolar E1/T1/J1 Tip		Analog	I
K2	RTIP_15	RPOS_15	Receive E1/T1/J1 serial data	I	LVCMOS	I
		RTIP_15	Receive Bipolar E1/T1/J1 Tip		Analog	I
J2	RTIP_16	RPOS_16	Receive E1/T1/J1 serial data	I	LVCMOS	I
		RTIP_16	Receive Bipolar E1/T1/J1 Tip		Analog	I

Ball Location	Ball Alias	Signal Name	Description	Reset State	Type	Dir.
H2	RTIP_17	RPOS_17	Receive E1/T1/J1 serial data	I	LVCMOS	I
		RTIP_17	Receive Bipolar E1/T1/J1 Tip		Analog	I
F2	RTIP_18	RPOS_18	Receive E1/T1/J1 serial data	I	LVCMOS	I
		RTIP_18	Receive Bipolar E1/T1/J1 Tip		Analog	I
E2	RTIP_19	RPOS_19	Receive E1/T1/J1 serial data	I	LVCMOS	I
		RTIP_19	Receive Bipolar E1/T1/J1 Tip		Analog	I
D2	RTIP_20	RPOS_20	Receive E1/T1/J1 serial data	I	LVCMOS	I
		RTIP_20	Receive Bipolar E1/T1/J1 Tip		Analog	I
AK5	RRING_0	RCLK_0	Receive E1/T1/J1 clock input	I	LVCMOS	I
		RRING_0	Receive Bipolar E1/T1/J1 Ring		Analog	I
AJ5	RRING_1	RCLK_1	Receive E1/T1/J1 clock input	I	LVCMOS	I
		RRING_1	Receive Bipolar E1/T1/J1 Ring		Analog	I
AH5	RRING_2	RCLK_2	Receive E1/T1/J1 clock input	I	LVCMOS	I
		RRING_2	Receive Bipolar E1/T1/J1 Ring		Analog	I
AF5	RRING_3	RCLK_3	Receive E1/T1/J1 clock input	I	LVCMOS	I
		RRING_3	Receive Bipolar E1/T1/J1 Ring		Analog	I
AE5	RRING_4	RCLK_4	Receive E1/T1/J1 clock input	I	LVCMOS	I
		RRING_4	Receive Bipolar E1/T1/J1 Ring		Analog	I
AD5	RRING_5	RCLK_5	Receive E1/T1/J1 clock input	I	LVCMOS	I
		RRING_5	Receive Bipolar E1/T1/J1 Ring		Analog	I
AB5	RRING_6	RCLK_6	Receive E1/T1/J1 clock input	I	LVCMOS	I
		RRING_6	Receive Bipolar E1/T1/J1 Ring		Analog	I
AA5	RRING_7	RCLK_7	Receive E1/T1/J1 clock input	I	LVCMOS	I
		RRING_7	Receive Bipolar E1/T1/J1 Ring		Analog	I
Y5	RRING_8	RCLK_8	Receive E1/T1/J1 clock input	I	LVCMOS	I
		RRING_8	Receive Bipolar E1/T1/J1 Ring		Analog	I
V1	RRING_9	RCLK_9	Receive E1/T1/J1 clock input	I	LVCMOS	I
		RRING_9	Receive Bipolar E1/T1/J1 Ring		Analog	I
U1	RRING_10	RCLK_10	Receive E1/T1/J1 clock input	I	LVCMOS	I
		RRING_10	Receive Bipolar E1/T1/J1 Ring		Analog	I
T1	RRING_11	RCLK_11	Receive E1/T1/J1 clock input	I	LVCMOS	I
		RRING_11	Receive Bipolar E1/T1/J1 Ring		Analog	I
P1	RRING_12	RCLK_12	Receive E1/T1/J1 clock input	I	LVCMOS	I
		RRING_12	Receive Bipolar E1/T1/J1 Ring		Analog	I
N1	RRING_13	RCLK_13	Receive E1/T1/J1 clock input	I	LVCMOS	I
		RRING_13	Receive Bipolar E1/T1/J1 Ring		Analog	I
M1	RRING_14	RCLK_14	Receive E1/T1/J1 clock input	I	LVCMOS	I
		RRING_14	Receive Bipolar E1/T1/J1 Ring		Analog	I
K1	RRING_15	RCLK_15	Receive E1/T1/J1 clock input	I	LVCMOS	I
		RRING_15	Receive Bipolar E1/T1/J1 Ring		Analog	I

Ball Location	Ball Alias	Signal Name	Description	Reset State	Type	Dir.
J1	RRING_16	RCLK_16	Receive E1/T1/J1 clock input	I	LVCMOS	I
		RRING_16	Receive Bipolar E1/T1/J1 Ring		Analog	I
H1	RRING_17	RCLK_17	Receive E1/T1/J1 clock input	I	LVCMOS	I
		RRING_17	Receive Bipolar E1/T1/J1 Ring		Analog	I
F1	RRING_18	RCLK_18	Receive E1/T1/J1 clock input	I	LVCMOS	I
		RRING_18	Receive Bipolar E1/T1/J1 Ring		Analog	I
E1	RRING_19	RCLK_19	Receive E1/T1/J1 clock input	I	LVCMOS	I
		RRING_19	Receive Bipolar E1/T1/J1 Ring		Analog	I
D1	RRING_20	RCLK_20	Receive E1/T1/J1 clock input	I	LVCMOS	I
		RRING_20	Receive Bipolar E1/T1/J1 Ring		Analog	I
AK1	TTIP_0	TPOS_0	Transmit E1/T1/J1 serial data	O	LVCMOS	O
		TTIP_0	Transmit Bipolar E1/T1/J1 Tip		Analog	O
AJ1	TTIP_1	TPOS_1	Transmit E1/T1/J1 serial data	O	LVCMOS	O
		TTIP_1	Transmit Bipolar E1/T1/J1 Tip		Analog	O
AH1	TTIP_2	TPOS_2	Transmit E1/T1/J1 serial data	O	LVCMOS	O
		TTIP_2	Transmit Bipolar E1/T1/J1 Tip		Analog	O
AF1	TTIP_3	TPOS_3	Transmit E1/T1/J1 serial data	O	LVCMOS	O
		TTIP_3	Transmit Bipolar E1/T1/J1 Tip		Analog	O
AE1	TTIP_4	TPOS_4	Transmit E1/T1/J1 serial data	O	LVCMOS	O
		TTIP_4	Transmit Bipolar E1/T1/J1 Tip		Analog	O
AD1	TTIP_5	TPOS_5	Transmit E1/T1/J1 serial data	O	LVCMOS	O
		TTIP_5	Transmit Bipolar E1/T1/J1 Tip		Analog	O
AB1	TTIP_6	TPOS_6	Transmit E1/T1/J1 serial data	O	LVCMOS	O
		TTIP_6	Transmit Bipolar E1/T1/J1 Tip		Analog	O
AA1	TTIP_7	TPOS_7	Transmit E1/T1/J1 serial data	O	LVCMOS	O
		TTIP_7	Transmit Bipolar E1/T1/J1 Tip		Analog	O
Y1	TTIP_8	TPOS_8	Transmit E1/T1/J1 serial data	O	LVCMOS	O
		TTIP_8	Transmit Bipolar E1/T1/J1 Tip		Analog	O
V5	TTIP_9	TPOS_9	Transmit E1/T1/J1 serial data	O	LVCMOS	O
		TTIP_9	Transmit Bipolar E1/T1/J1 Tip		Analog	O
U5	TTIP_10	TPOS_10	Transmit E1/T1/J1 serial data	O	LVCMOS	O
		TTIP_10	Transmit Bipolar E1/T1/J1 Tip		Analog	O
T5	TTIP_11	TPOS_11	Transmit E1/T1/J1 serial data	O	LVCMOS	O
		TTIP_11	Transmit Bipolar E1/T1/J1 Tip		Analog	O
P5	TTIP_12	TPOS_12	Transmit E1/T1/J1 serial data	O	LVCMOS	O
		TTIP_12	Transmit Bipolar E1/T1/J1 Tip		Analog	O
N5	TTIP_13	TPOS_13	Transmit E1/T1/J1 serial data	O	LVCMOS	O
		TTIP_13	Transmit Bipolar E1/T1/J1 Tip		Analog	O
M5	TTIP_14	TPOS_14	Transmit E1/T1/J1 serial data	O	LVCMOS	O
		TTIP_14	Transmit Bipolar E1/T1/J1 Tip		Analog	O

Ball Location	Ball Alias	Signal Name	Description	Reset State	Type	Dir.
K5	TTIP_15	TPOS_15	Transmit E1/T1/J1 serial data	O	LVCMOS	O
		TTIP_15	Transmit Bipolar E1/T1/J1 Tip		Analog	O
J5	TTIP_16	TPOS_16	Transmit E1/T1/J1 serial data	O	LVCMOS	O
		TTIP_16	Transmit Bipolar E1/T1/J1 Tip		Analog	O
H5	TTIP_17	TPOS_17	Transmit E1/T1/J1 serial data	O	LVCMOS	O
		TTIP_17	Transmit Bipolar E1/T1/J1 Tip		Analog	O
F5	TTIP_18	TPOS_18	Transmit E1/T1/J1 serial data	O	LVCMOS	O
		TTIP_18	Transmit Bipolar E1/T1/J1 Tip		Analog	O
E5	TTIP_19	TPOS_19	Transmit E1/T1/J1 serial data	O	LVCMOS	O
		TTIP_19	Transmit Bipolar E1/T1/J1 Tip		Analog	O
D5	TTIP_20	TPOS_20	Transmit E1/T1/J1 serial data	O	LVCMOS	O
		TTIP_20	Transmit Bipolar E1/T1/J1 Tip		Analog	O
AK2	TRING_0	TCLK_0	Transmit E1/T1/J1 clock output	O	LVCMOS	O
		TRING_0	Transmit Bipolar E1/T1/J1 Ring		Analog	O
AJ2	TRING_1	TCLK_1	Transmit E1/T1/J1 clock output	O	LVCMOS	O
		TRING_1	Transmit Bipolar E1/T1/J1 Ring		Analog	O
AH2	TRING_2	TCLK_2	Transmit E1/T1/J1 clock output	O	LVCMOS	O
		TRING_2	Transmit Bipolar E1/T1/J1 Ring		Analog	O
AF2	TRING_3	TCLK_3	Transmit E1/T1/J1 clock output	O	LVCMOS	O
		TRING_3	Transmit Bipolar E1/T1/J1 Ring		Analog	O
AE2	TRING_4	TCLK_4	Transmit E1/T1/J1 clock output	O	LVCMOS	O
		TRING_4	Transmit Bipolar E1/T1/J1 Ring		Analog	O
AD2	TRING_5	TCLK_5	Transmit E1/T1/J1 clock output	O	LVCMOS	O
		TRING_5	Transmit Bipolar E1/T1/J1 Ring		Analog	O
AB2	TRING_6	TCLK_6	Transmit E1/T1/J1 clock output	O	LVCMOS	O
		TRING_6	Transmit Bipolar E1/T1/J1 Ring		Analog	O
AA2	TRING_7	TCLK_7	Transmit E1/T1/J1 clock output	O	LVCMOS	O
		TRING_7	Transmit Bipolar E1/T1/J1 Ring		Analog	O
Y2	TRING_8	TCLK_8	Transmit E1/T1/J1 clock output	O	LVCMOS	O
		TRING_8	Transmit Bipolar E1/T1/J1 Ring		Analog	O
V4	TRING_9	TCLK_9	Transmit E1/T1/J1 clock output	O	LVCMOS	O
		TRING_9	Transmit Bipolar E1/T1/J1 Ring		Analog	O
U4	TRING_10	TCLK_10	Transmit E1/T1/J1 clock output	O	LVCMOS	O
		TRING_10	Transmit Bipolar E1/T1/J1 Ring		Analog	O
T4	TRING_11	TCLK_11	Transmit E1/T1/J1 clock output	O	LVCMOS	O
		TRING_11	Transmit Bipolar E1/T1/J1 Ring		Analog	O
P4	TRING_12	TCLK_12	Transmit E1/T1/J1 clock output	O	LVCMOS	O
		TRING_12	Transmit Bipolar E1/T1/J1 Ring		Analog	O
N4	TRING_13	TCLK_13	Transmit E1/T1/J1 clock output	O	LVCMOS	O
		TRING_13	Transmit Bipolar E1/T1/J1 Ring		Analog	O

Ball Location	Ball Alias	Signal Name	Description	Reset State	Type	Dir.
M4	TRING_14	TCLK_14	Transmit E1/T1/J1 clock output	O	LVCMOS	O
		TRING_14	Transmit Bipolar E1/T1/J1 Ring		Analog	O
K4	TRING_15	TCLK_15	Transmit E1/T1/J1 clock output	O	LVCMOS	O
		TRING_15	Transmit Bipolar E1/T1/J1 Ring		Analog	O
J4	TRING_16	TCLK_16	Transmit E1/T1/J1 clock output	O	LVCMOS	O
		TRING_16	Transmit Bipolar E1/T1/J1 Ring		Analog	O
H4	TRING_17	TCLK_17	Transmit E1/T1/J1 clock output	O	LVCMOS	O
		TRING_17	Transmit Bipolar E1/T1/J1 Ring		Analog	O
F4	TRING_18	TCLK_18	Transmit E1/T1/J1 clock output	O	LVCMOS	O
		TRING_18	Transmit Bipolar E1/T1/J1 Ring		Analog	O
E4	TRING_19	TCLK_19	Transmit E1/T1/J1 clock output	O	LVCMOS	O
		TRING_19	Transmit Bipolar E1/T1/J1 Ring		Analog	O
D4	TRING_20	TCLK_20	Transmit E1/T1/J1 clock output	O	LVCMOS	O
		TRING_20	Transmit Bipolar E1/T1/J1 Ring		Analog	O
AM4	MCLK	MCLK	E1/T!/J1 reference clock (32.768MHz or 24.704MHz)	I	LVCMOS Input	I
AL1	R_REF_0	R_REF_0	Reference resistors connection pin for the internal LIU		Analog	
R1	R_REF_12	R_REF_12			Analog	
G1	R_REF_17	R_REF_17			Analog	
AM2	ACLK	ACLK	E1/T1/J1 MCLK output	I	LVCMOS I/O, 12ma	O

2.4 PVG610X Exclusive Signals Pin List

Ball Location	Ball Alias	Signal Name	Description	Reset State	Buffer Type	Dir.
AK4	RTIP_0	RPOS_0	Receive E1/T1/J1 serial data	I	LVCMOS	I
		RTIP_0	Receive Bipolar E1/T1/J1 Tip		Analog	
AJ4	RTIP_1	RPOS_1	Receive E1/T1/J1 serial data	I	LVCMOS	I
		RTIP_1	Receive Bipolar E1/T1/J1 Tip		Analog	I
AK5	RRING_0	RCLK_0	Receive E1/T1/J1 clock input	I	LVCMOS	I
		RRING_0	Receive Bipolar E1/T1/J1 Ring		Analog	I
AJ5	RRING_1	RCLK_1	Receive E1/T1/J1 clock input	I	LVCMOS	I
		RRING_1	Receive Bipolar E1/T1/J1 Ring		Analog	I
AK1	TTIP_0	TPOS_0	Transmit E1/T1/J1 serial data	O	LVCMOS	O
		TTIP_0	Transmit Bipolar E1/T1/J1 Tip		Analog	O
AJ1	TTIP_1	TPOS_1	Transmit E1/T1/J1 serial data	O	LVCMOS	O
		TTIP_1	Transmit Bipolar E1/T1/J1 Tip		Analog	O
AK2	TRING_0	TCLK_0	Transmit E1/T1/J1 clock output	O	LVCMOS	O
		TRING_0	Transmit Bipolar E1/T1/J1 Ring		Analog	O
AJ2	TRING_1	TCLK_1	Transmit E1/T1/J1 clock output	O	LVCMOS	O
		TRING_1	Transmit Bipolar E1/T1/J1 Ring		Analog	O
AM4	MCLK	MCLK	E1/T!/J1 reference clock (32.768MHz or 24.704MHz)	I	LVCMOS Input	I
AL1	R_REF_0	R_REF_0	Reference resistor connection pin for the internal LIU		Analog	
AM2	ACLK	ACLK	E1/T1/J1 MCLK output	I	LVCMOS I/O, 12ma	O
V5	SYMI_0	SYMI_0	XPIC master symbol[23:0] input	I	LVCMOS I/O, 8ma	I
		SYMO_0	XPIC slave symbol[23:0] output			O
AB1	SYMI_1	SYMI_1			LVCMOS I/O, 8ma	I
		SYMO_1				O
AA1	SYMI_2	SYMI_2_			LVCMOS I/O, 8ma	I
		SYMO_2				O
Y1	SYMI_3	SYMI_3			LVCMOS I/O, 8ma	I
		SYMO_3				O
AD4	SYMI_4	SYMI_4			LVCMOS I/O, 8ma	I
		SYMO_4				O
AD2	SYMI_5	SYMI_5			LVCMOS I/O, 8ma	I
		SYMO_5				O
AD1	SYMI_6	SYMI_6			LVCMOS I/O, 8ma	I
		SYMO_6				O
AB5	SYMI_7	SYMI_7			LVCMOS I/O, 8ma	I
		SYMO_7				O
AB4	SYMI_8	SYMI_8			LVCMOS	I

Ball Location	Ball Alias	Signal Name	Description	Reset State	Buffer Type	Dir.
		SYMO_8			I/O, 8ma	O
AB2	SYMI_9	SYMI_9			LVCMOS I/O, 8ma	I
		SYMO_9				O
AA5	SYMI_10	SYMI_10			LVCMOS I/O, 8ma	I
		SYMO_10				O
AA4	SYMI_11	SYMI_11			LVCMOS I/O, 8ma	I
		SYMO_11				O
AA2	SYMI_12	SYMI_12			LVCMOS I/O, 8ma	I
		SYMO_12				O
Y4	SYMI_13	SYMI_13			LVCMOS I/O, 8ma	I
		SYMO_13				O
Y2	SYMI_14	SYMI_14			LVCMOS I/O, 8ma	I
		SYMO_14				O
V1	SYMI_15	SYMI_15			LVCMOS I/O, 8ma	I
		SYMO_15				O
V2	SYMI_16	SYMI_16			LVCMOS I/O, 8ma	I
		SYMO_16				O
V4	SYMI_17	SYMI_17			LVCMOS I/O, 8ma	I
		SYMO_17				O
U1	SYMI_18	SYMI_18			LVCMOS I/O, 8ma	I
		SYMO_18				O
U2	SYMI_19	SYMI_19			LVCMOS I/O, 8ma	I
		SYMO_19				O
U4	SYMI_20	SYMI_20			LVCMOS I/O, 8ma	I
		SYMO_20				O
T1	SYMI_21	SYMI_21			LVCMOS I/O, 8ma	I
		SYMO_21				O
T2	SYMI_22	SYMI_22			LVCMOS I/O, 8ma	I
		SYMO_22				O
T4	SYMI_23	SYMI_23			LVCMOS I/O, 8ma	I
		SYMO_23				O
Y5	SYMI_STROBE	SYMI_STROBE	XPIC master symbol Strobe input XPIC slave symbol Strobe output		LVCMOS I/O, 12ma	I
		SYMO_STROBE				O
N5	ERRO_0	ERRO_0	XPIC master Error[9:0] output XPIC slave Error[9:0] input		LVCMOS I/O, 8ma	O
		ERRI_0				I
U5	ERRO_1	ERRO_1			LVCMOS I/O, 8ma	O
		ERRI_1				I
M5	ERRO_2	ERRO_2			LVCMOS I/O, 8ma	O
		ERRI_2				I

Ball Location	Ball Alias	Signal Name	Description	Reset State	Buffer Type	Dir.
T5	ERRO_3	ERRO_3			LVCMOS I/O, 8ma	O
		ERRI_3				I
K4	ERRO_4	ERRO_4			LVCMOS I/O, 8ma	O
		ERRI_4				I
K5	ERRO_5	ERRO_5			LVCMOS I/O, 8ma	O
		ERRI_5				I
P5	ERRO_6	ERRO_6			LVCMOS I/O, 8ma	O
		ERRI_6				I
J4	ERRO_7	ERRO_7			LVCMOS I/O, 8ma	O
		ERRI_7				I
J5	ERRO_8	ERRO_8			LVCMOS I/O, 8ma	O
		ERRI_8				I
P4	ERRO_9	ERRO_9			LVCMOS I/O, 8ma	O
		ERRI_9				I
N4	ERRO_STROBE	ERRO_STROBE	XPIC master Error Strobe output		LVCMOS I/O, 12ma	O
		ERRI_STROBE	XPIC slave Error Strobe input			I
M4	ERRO_PILOT	ERRO_PILOT	XPIC master Error Pilot output		LVCMOS I/O, 8ma	O
		ERRI_PILOT	XPIC slave Error Pilot input			I
M1	TIMO_CALC	TIMO_CALC	XPIC Master Timing CALC Output		LVCMOS I/O, 12ma	O
		TIMI_CALC	XPIC Slave Timing CALC Input			I
K1	TIMO_GET	TIMO_GET	XPIC Master Timing GET Output		LVCMOS I/O, 12ma	O
		TIMI_GET	XPIC Slave Timing GET Input			I
P1	TIMO_MU_0	TIMO_MU_0	XPIC Master Timing MU[6:0] Output XPIC Slave Timing MU[6:0] Input		LVCMOS I/O, 12ma	O
		TIMI_MU_0				I
P2	TIMO_MU_1	TIMO_MU_1			LVCMOS I/O, 12ma	O
		TIMI_MU_1				I
N2	TIMO_MU_2	TIMO_MU_2			LVCMOS I/O, 12ma	O
		TIMI_MU_2				I
M2	TIMO_MU_3	TIMO_MU_3			LVCMOS I/O, 12ma	O
		TIMI_MU_3				I
K2	TIMO_MU_4	TIMO_MU_4			LVCMOS I/O, 12ma	O
		TIMI_MU_4				I
J1	TIMO_MU_5	TIMO_MU_5			LVCMOS I/O, 12ma	O
		TIMI_MU_5				I
J2	TIMO_MU_6	TIMO_MU_6			LVCMOS I/O, 12ma	O
		TIMI_MU_6				I
N1	TIM_GET_OUT	Reserved	Should be left unconnected			

Ball Location	Ball Alias	Signal Name	Description	Reset State	Buffer Type	Dir.
AD5/AE1/AE2/AE4/AE5/AF1/AF2/AF4/AF5/AH1/AH2/ AH4/AH5/D1/D2/D4/D5/E1/E2/E4/E5/F1/F2/F4/F5/G1/ H1/H2/H4/H5/R1			Not connected			

2.5 PVG610A and PVG610X Common Power/Ground Pin List

Alias / Signal Name	Power Ground	Ball Location
ADC_CLK_VDD1P2	Power	D23
ADC_VDD1P2	Power	C20/C21/C22/C23/C24/C25
ADC_VDD3P3	Power	C19
DAC_CLK_VDD1P2	Power	D10
DAC_VDD1P2	Power	C15/C16/C17/C18/D16/D18/E15/E17
DAC_VDD3P3	Power	C10/C11/C12/C13/C14/C8/C9/D12/D14/D8/E11/E13
LIU_VDD3P3	Power	AB3/AC3/AC5/AD3/AF3/AG3/AG5/AH3/AK3/AL3/C1/C3/D3/F3/G3/G5/H3 /K3/L3/L5/M3/P3/R3/R5/T3/V3/W3/W5/Y3
PLL_VDDA1P2	Power	P13
SYS_CLK_VDD1P2	Power	N15
VDD1P2	Power	AA13/AA22/AB13/AB14/AB15/AB16/AB17/AB18/AB19/AB20/AB21/AB22/ N16/N17/N18/N19/N20/N21/N22/P22/R13/R22/T13/T22/U13/U22/V13/V2 2/W13/W22/Y13/Y22
VDD3P3	Power	A32/A33/A34/AB33/AC31/AF33/AG31/AK30/AK33/AL11/AL15/AL22/AL2 6/AL31/AL7/AM32/AN12/AN18/AN23/AN27/AN33/AN34/AN8/AP2/AP3/A P33/AP34/B33/C31/F33/G31/K33/L31/P33/R31/V33/W31
ADC_CLK_VSS	Ground	D22
ADC_VSS[1]	Ground	A19/A22/A23/A26/A27/B19/B21/B22/B23/B25/B26/B27/C26/D19/D21/D2 4/D25/E19/E21/E24
DAC_CLK_VSS	Ground	D9
DAC_VSS[2]	Ground	A10/A11/A14/A15/A18/A7/B10/B12/B13/B14/B15/B17/B18/B7/B8/B9/C7/ D11/D13/D15/D17/D7/E12/E14/E16/E18/E7/E8
PLL_VSSA	Ground	N13
SYS_CLK_VSS	Ground	N14
VSS[3]	Ground	A1/A2/A5/AA14/AA15/AA16/AA17/AA18/AA19/AA20/AA21/AA3/AA31/AC 1/AC2/AC4/AD33/AE3/AE31/AG1/AG2/AG4/AH33/AJ3/AJ31/AK6/AL13/A L19/AL2/AL24/AL28/AL4/AL5/AL9/AM1/AM3/AM34/AN1/AN10/AN14/AN 2/AN21/AN25/AN30/AN6/AP1/B1/B2/B29/B3/B34/B4/B5/C2/C34/C4/C5/ D33/D6/E3/E31/E6/G2/G4/H33/J3/J31/L1/L2/L4/M33/N3/N31/P14/P15/P 16/P17/P18/P19/P20/P21/R14/R15/R16/R17/R18/R19/R2/R20/R21/R4/T 14/T15/T16/T17/T18/T19/T20/T21/T33/U14/U15/U16/U17/U18/U19/U20/ U21/U3/U31/V14/V15/V16/V17/V18/V19/V20/V21/W1/W14/W15/W16/W1 7/W18/W19/W2/W20/W21/W4/Y14/Y15/Y16/Y17/Y18/Y19/Y20/Y21/Y33

1. ADC_VSS is the ground pin for ADC_VDD1P2 and ADC_VDD3P3 voltage sources.
2. DAC_VSS is the ground pin for DAC_VDD1P2 and DAC_VDD3P3 voltage sources.
3. VSS is the ground pin for VDD1P2, VDD3P3 and LIU_VDD3P3 voltage sources.

2.6 Pin Compatibility between PVG610A and PVG610X

The following table lists the pins that have different functionality between the PVG610A and PVG610X.

PVG610A Functionality	PVG610X Functionality	Ball Location
TTIP/TRING	SYMO/I	AB1, AA1, Y1, V5, AD2, AD1, AB2, AA2, Y2, V4, U4, T4,
RTIP/RRING	SYMO/I	AD4, AB5, AB4, AA4, AA5, Y4, V2, V1, U1, U2, T1, T2
RRING	SYM STROBE	Y5
TTIP/TRING	ERRO/I	N5, M5, U5, T5, K5, K4, P4, J4, J5, P5,
TRING	ERR STROBE	N4
TRING	ERR PILOT	M4
RTIP/RRING	TIMO MU	M2, N2, P2, P1, J1, J2, K2
RRING	TIMO CALC	M1
RRING	TIMO GET	K1
RRING	TIM GET OUT	N1
RTIP/RRING	Not connected	AH4, AF4, AE4, H2, F2, E2, D2, AH5, AF5, AE5, AD5, H1, F1, E1, D1
TTIP/TRING	Not connected	AH1, AE1, AF1, H5, F5, D5, E5, AF2, AE2, AH2, H4, F4, D4, E4
RREF12/17	not connected	R1, G1

The two devices are inter-replaceable as long as the pins listed above are left unconnected or pulled up or pulled down.

3 Functional Description

This chapter provides an overview of PVG610A and functional description of its main functional blocks.

3.1 PVG610A Block Diagram Overview

Below is a block diagram of the PVG610A showing its main functional blocks, followed by highlights of the data flow.

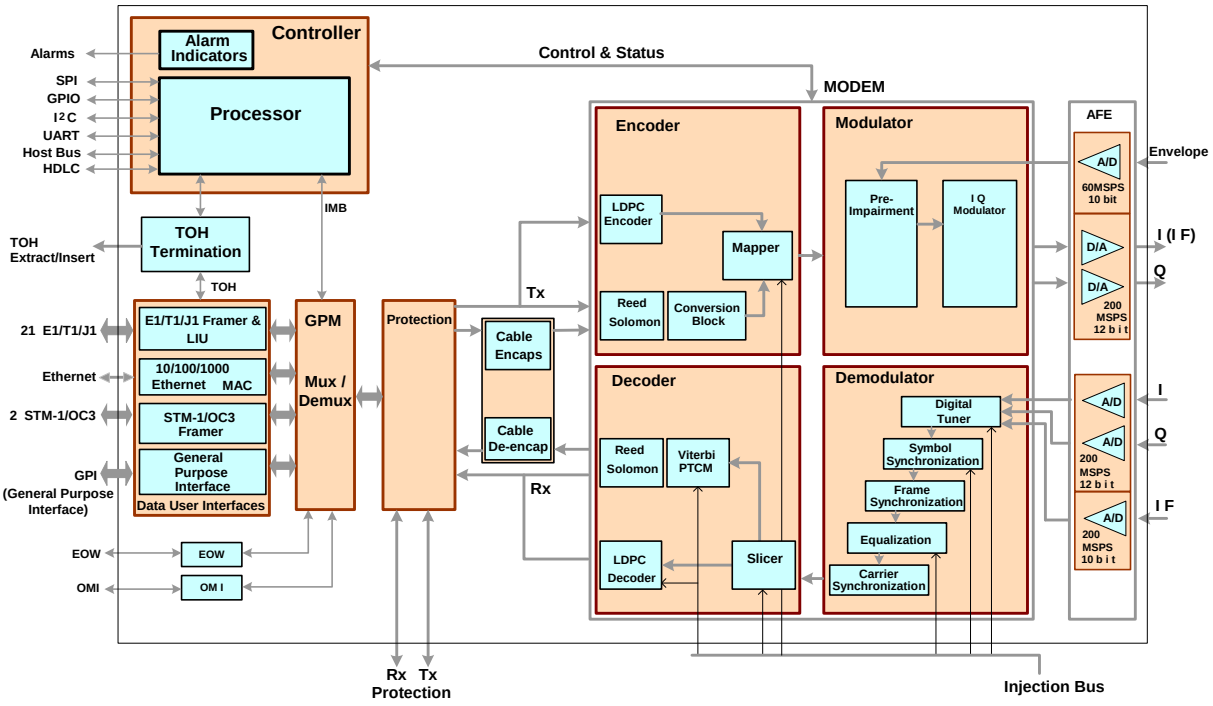


***Figure 6: PVG610A* Block Diagram**

Users can interface to the PVG610A with a variety of data transport types including; 21 E1/T1 ports, an Ethernet port, 2 STM-1/OC-3 ports and a proprietary General Purpose Interface (GPI) port. The diagram shows the flow from the user interface to the Analog Front End and back.

In the transmit direction user data is extracted from the physical interface and transferred to the General Purpose Multiplexer (GPM). The GPM organizes data from multiple sources, builds data frames to be transmitted and sends the frames to the protection block. The protection block serves as a switching matrix. It enables transferring the local GPM frames to a modem in another board or to transfer GPM frames from another board to the local modem. The modem encodes and modulates the data and transfers digital words to the Analog Front End (AFE). The AFE generates the IF or Base-Band analog signal for transmission.

On the receive side the AFE receives the IF or the Base-Band analog signal, converts it to a digital format and sends it to the modem. The modem demodulates and decodes the data and passes it to the protection block. The protection block may transfer the modem data to another board or receive modem data from another board. In the later case the protection block selects the data with less number of errors and passes it to the GPM. The GPM extracts the different data types from the GPM frame and distributes the extracted data to the addressed user interfaces.

3.2 User Interface Block

The user interface block has interfaces to the following types of data links:

- E1/T1/J1
- Ethernet 10/100/1000
- STM-1/OC-3
- GPI
- EOW
- OMI

3.2.1 E1/T1/J1 Interface Block

The PVG610A E1/T1/J1 block supports 21 user ports of E1/T1/J1 links.

The following features are supported:

- Integrated or external Line Interface Unit (LIU).
- E1/T1/J1 framing
- Jitter attenuation
- Alarms and performance monitoring
- PRBS injection/analysis
- Support AIS and RAI forced insertion toward line and radio direction

The following figure illustrates a typical E1/T1/J1 line connection to the PVG610A using its internal LIU.

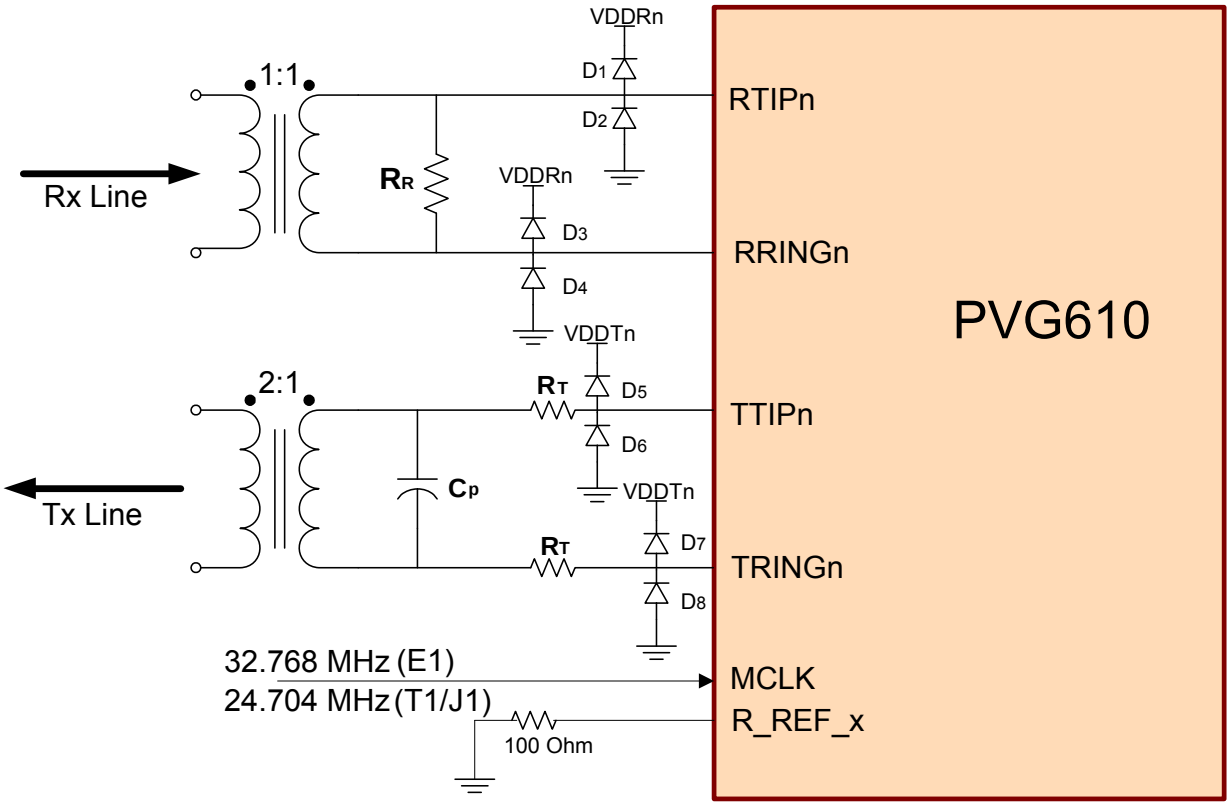


Figure 7: E1/T1 Port Connection

3.2.1.1 Block Diagram Description

Receive Path

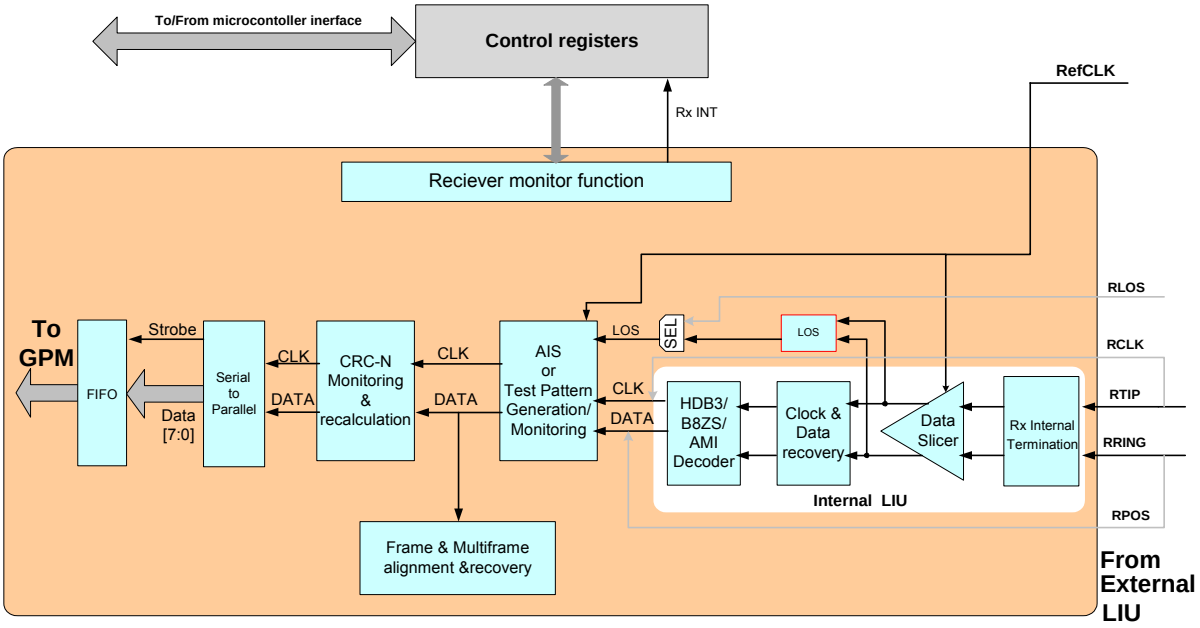


Figure 8: Rx E1/T1/J1 LIU/Framer Block

The digital signal (data and Clock) enters an alignment block for detecting the beginning of the E1/T1/J1 frame. When frame alignment and multi frame alignment is completed, data is monitored for alarms (LOF, RAI, LMFAS, LSMFA and LCMFA) and performance monitoring (CRC-N, Excessive CRC errors, Far End Block Errors, etc). There is an option to generate/monitor PRBS before data is sent to the GPM. The serial data is then converted to a parallel/byte as it continues to the GPM.

Note:

When an external LIU is used, the digital signal bypasses (broken lines) the internal LIU and enters the E1/T1/J1 framer as an output of the Internal LIU.

Transmit Path

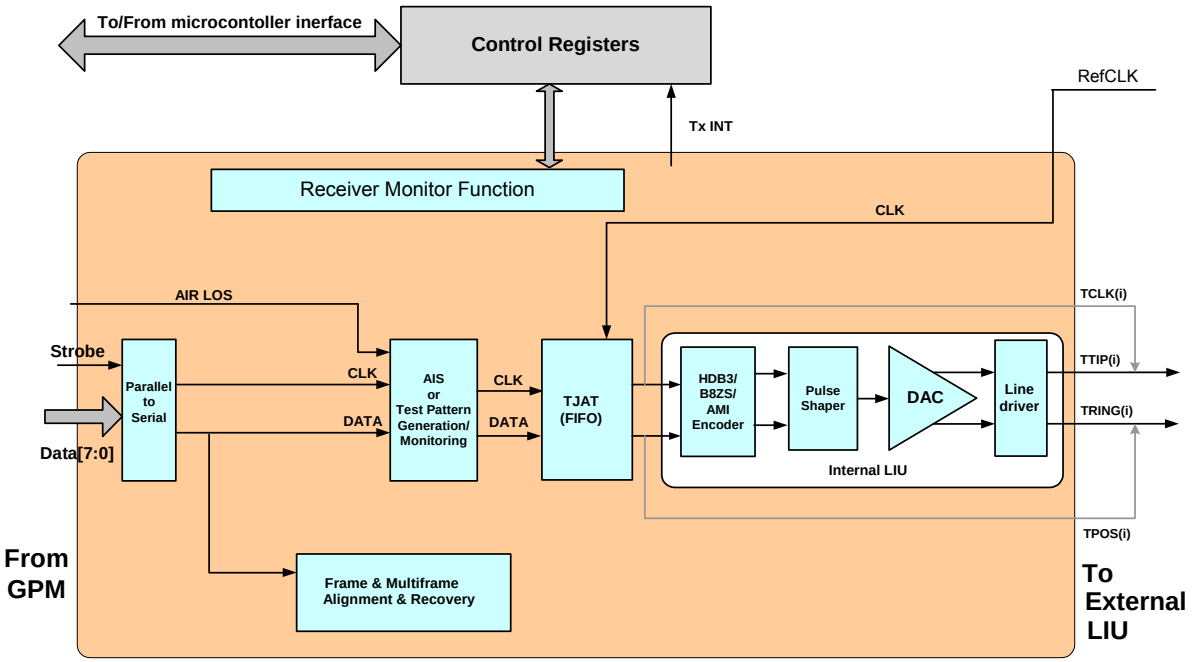


***Figure 9**: Tx E1/T1/J1 LIU/Framer Block*

Parallel data passes a byte-to-serial conversion block before going to the E1/T1/J1 framer the digital serial stream (data and clock) enters the alignment block to search for the beginning of the E1/T1/J1 frame. An option to generate/monitor PRBS exists before data is sent to the TJAT. The serial data passes a jitter attenuator (TJAT) and enters the internal LIU to convert from digital to analog signal (passing Encoder, pulse shaper DAC and line driver).

Note:

When an external LIU is used, the digital signal bypasses the internal LIU goes directly to the external LIU.

3.2.1.2 Integrated LIU

The PVG610A contains integrated LIU which supports 21 E1/T1/J1 lines.

On the receive path each LIU receiver front-end has a programmable internal line termination network supporting multiple line types with a single external matching resistor (100Ω/T1, 110Ω J1 twisted pair, 120Ω/ E1 twisted pair and 75Ω/ E1 coaxial lines are supported). A Data Slicer follows the matching circuit and generates a standard amplitude mark or a space according to the amplitude of the input signals. The Slicer determines the presence and polarity of the received pulses. The Slicer circuit has a built-in peak detector from which the slicing threshold is derived, i.e. the peak detector samples the received signal and determines its maximum value. The output of the Data Slicer is forwarded to the CDR (Clock & Data Recovery) unit. A Loss of Signal detector indicates the signal level being too low, or that there are insufficient transitions on the receive line. The LOS detector meets ITU G.775, ETS 300 233 and T1.231.

The transmitter front-end is comprised of a differential 6-bit DAC (sampling rate 24.704 MHz to 32.768 MHz) and a line driver. The DAC is generating a pulse shape according to the link type to ensure that the T1/E1 pulse template is met after the signal travels through different cable lengths or types. The following modes are supported:

- E1/75 Ω
- E1/120 Ω,
- T1/ 100Ω / 0-133 ft
- J1/ 110Ω / 0-133 ft

3.2.1.3 E1/T1/J1 Frame Description

A single E1 frame is 256 bits wide and is generated 8000 times a second (every 125 µsec). Each frame is grouped into 32 octets or timeslots. These timeslots are numbered 0 to 31.

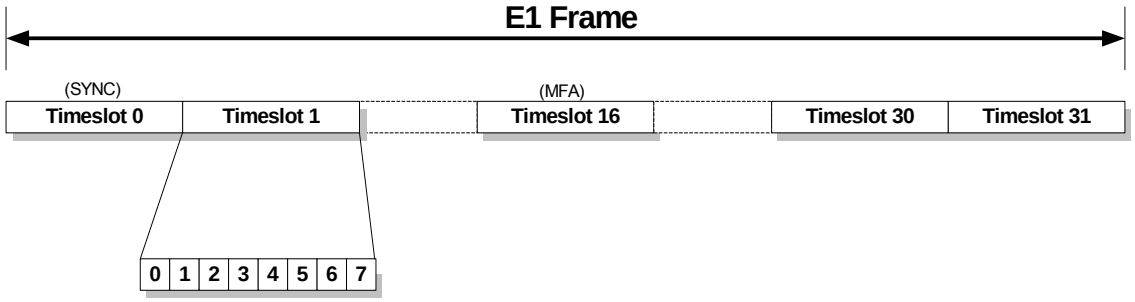


Figure *10: E1 Frame Format*

In even frames, bits 1-7 of Timeslot-0 contain Frame Alignment Signal (FAS).

There are two types of E1 frames:

- Basic Frame (or non-CRC framing): In this type of framing, there is no error checking capability.
- Multi Frame: Consists of 16 consecutive E1 frames. Error checking is supported with CRC-4 (transferred in timeslot 0).

The PVG610A supports both E1's framing types.

A single T1 frame is 193 bits wide, created 8000 times a second (every 125 µsec). Each frame is grouped into 24 octets or timeslots and one bit for synchronization. These timeslots are numbered 0 to 23.

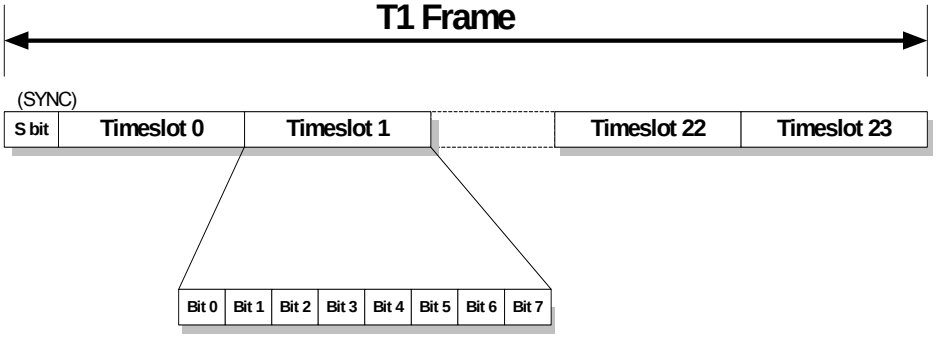


Figure 11: T1 Frame format

T1 support four types of framing:

- SF (D4) – Super frame, group of 12 frames
- ESF – Extended super frame, group of 24 frames. Error checking is supported with CRC-6.
- SLC-96 – similar to SF but group of 72 frames.
- T1DM (DDS) – similar to SF, but with timeslot 23 used for synchronization and PM
- The PVG610A supports the four T1's framing types.

J1 framing is similar to T1. However, SF and ESF frame types are supported.

All 21 E1/T1/J1 links in the PVG610A share the same reference clock. Thus, it is not possible to mix E1 links with T1/J1 links in the same application. However, mixing between different frame types of E1 or mixing between different frame types of T1/J1 is supported (i.e. each one of the 21 links can be configured to support a different framing type and cable length).

3.2.1.4 4 Alarms

The PVG610A identifies alarms and report about their appearance to the host SW via an interrupt mechanism. The following alarms are supported:

- Loss of Signal (LOS)
  - LOS from the line identified
  - Applicable for E1/T1/J1
  - AIS and RAI are injected as required by E1/T1/J1 standard (unless in manual control mode)
- Loss of Frame (LOF)
  - LOF from the line identified
  - Applicable for E1/T1/J1
  - AIS and RAI are injected as required by E1/T1/J1 standard (unless in manual control mode)
- Unframed Alarm Indication Signal (AIS)
  - Unframed AIS from the line identified
  - Applicable for E1/T1/J1
- TS16 Alarm Indication Signal (AIS)
  - TS16 AIS from the line identified
  - Applicable for E1
- Remote Alarm Indication (RAI)
  - RAI from the line identified
  - Applicable for E1/T1/J1
- Loss of Signaling Multiframe Alignment (LSMFA)
  - LSMFA from the line identified
  - Applicable for E1
- Loss of CRC Multiframe Alignment (LCMFA)
  - LCMFA from the line identified
  - Applicable for E1

3.2.1.5 Monitoring

The following events are monitored and counted by PVG610:

- Line code violations (LCV)
  - Applicable for E1/T1/J1 (when the PVG610A integrated LIU is used)
- CRC-N block errors
  - N=4 for E1 and N=6 for T1/J1
- Excessive CRC errors – E1/T1/J1
- Far End Block errors – Only for E1
- Framing alignment bit errors – E1/T1/J1

The monitoring is conducted on events from the line direction.

3.2.1.6 PRBS

PVG610A supports Pseudo-random bit sequence (PRBS) Generator and Monitor. It generates and monitors an unframed (215-1) payload test sequence in an E1/T1/J1 frame. The test sequence is inserted in the frames.

The generating polynomial is g(x) = X15 + X14 + 1.

The PRBS can be injected to the line or to the radio traffic. PRBS monitoring can be conducted on the line or radio traffic.

3.2.2 Ethernet Interface Block

The Ethernet port operates at 10, 100, or 1000 Mbps and supports a built-in MII/GMII interface. It is built of MAC, FIFOs and encapsulating/ de-encapsulating blocks.

The following features are supported:

Operates at 10, 100 or 1000 Mbps.

- 802.3x Full Duplex Flow Control; also supports Half Duplex when operating at 10 or 100 Mbps (with Back Pressure).
- 802.3ac (frame extension to 1522 bytes to allow Q-tag)
- Support of Jumbo frames (up to 10K bytes).
- MII/GMII interfaces.
- MII management interface (MDC/MDIO) for the physical layer management.
- Programmable automatic discard of erroneous frames, Broadcast/Multicast destination address.
- Programmable automatic pad and CRC generation on transmitted frames.
- Programmable IPG stretch.
- Support for 802.1Q VLAN tagging with recognition of incoming VLAN and user priority level bits.
- Support of transmit & receive statistics vectors, supporting RMON and SNMP.

The following figure illustrates a typical connection of Ethernet PHY to the PVG610.

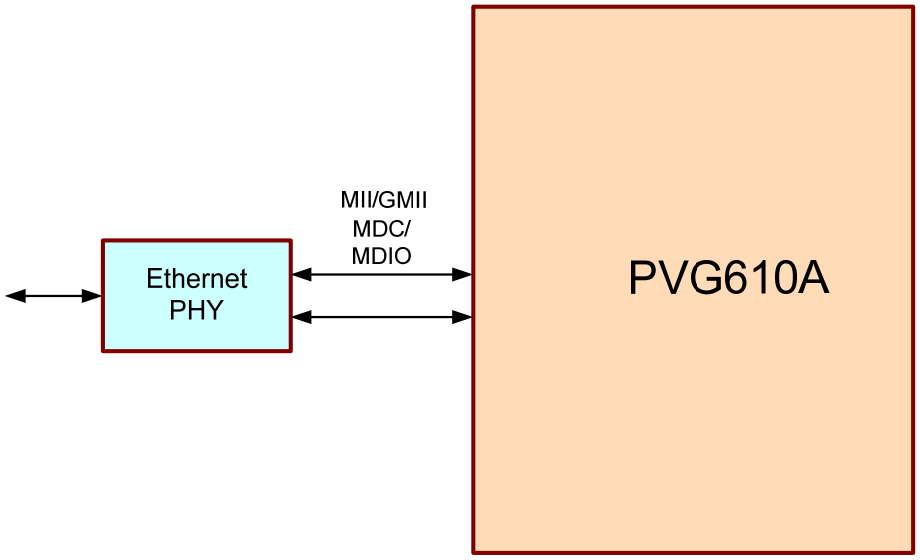


Figure 12: Ethernet PHY Connection

3.2.2.1 Block Diagram Description

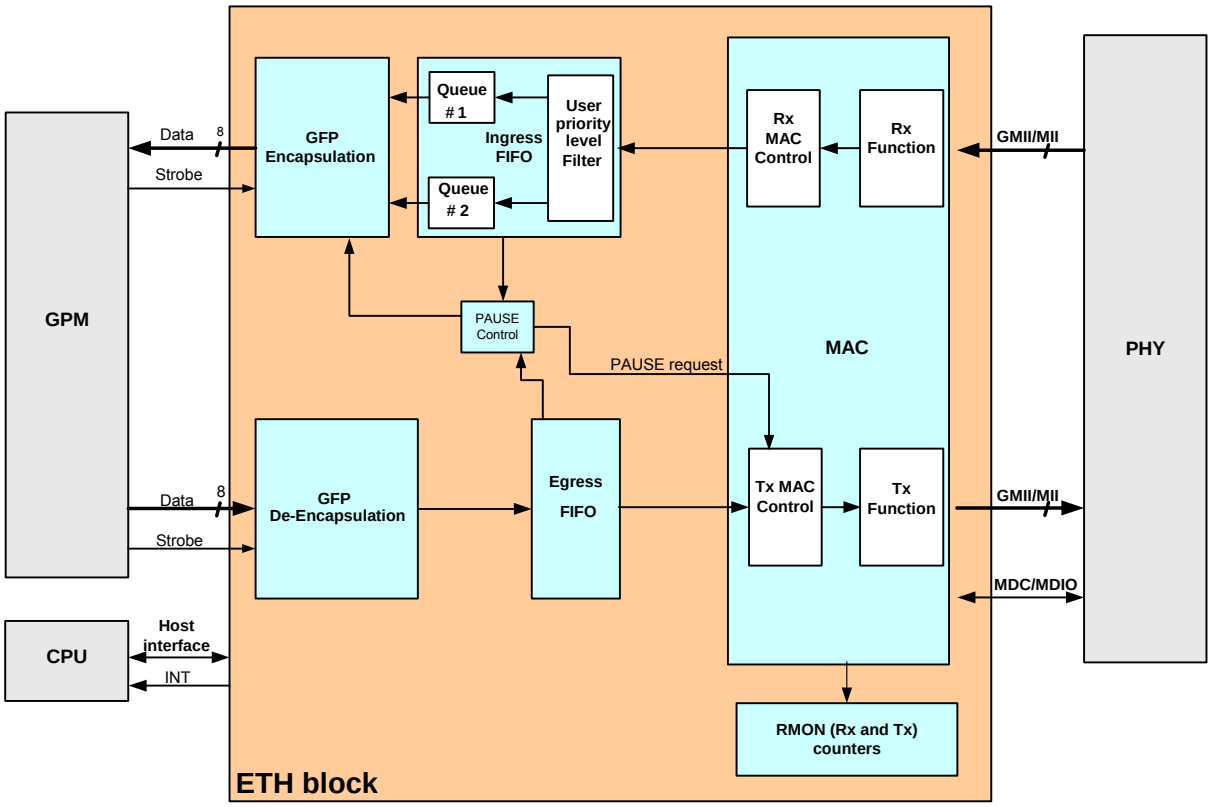


Figure 13: Ethernet Block Diagram

Receive Path:

The Rx MAC receives packets via the MII/GMII interface. It strips the preamble and the Start of Frame Delimiter from each frame before sending it to the relevant queues. Each Ethernet frame is checked for FCS error and then routed either through the high priority queue or the low priority queue (best effort) according to a predefined user priority level of VLAN frames. Each frame is then encapsulated as a Generic Framing Procedure (GFP) frame sent toward to the GPM.

Transmit Path:

Each GFP frame received from the GPM is de-encapsulated and routed to the transmit FIFO. The Ethernet frame enters the Tx MAC that builds the preamble and the Start of frame delimiter before sending it to the MII/GMII interface. When Inband flow control is enabled and the remote egress FIFO reaches WLH (Water Level High), the remote PVG610A sends a request using spare bits in the GFP OH, to send a PAUSE frame in the local PVG610A towards the ETH network, preventing egress remote FIFO overflow

3.2.2.2 Ethernet Frame

The figure below shows the different types of Ethernet frames (with and without VLAN tagging).

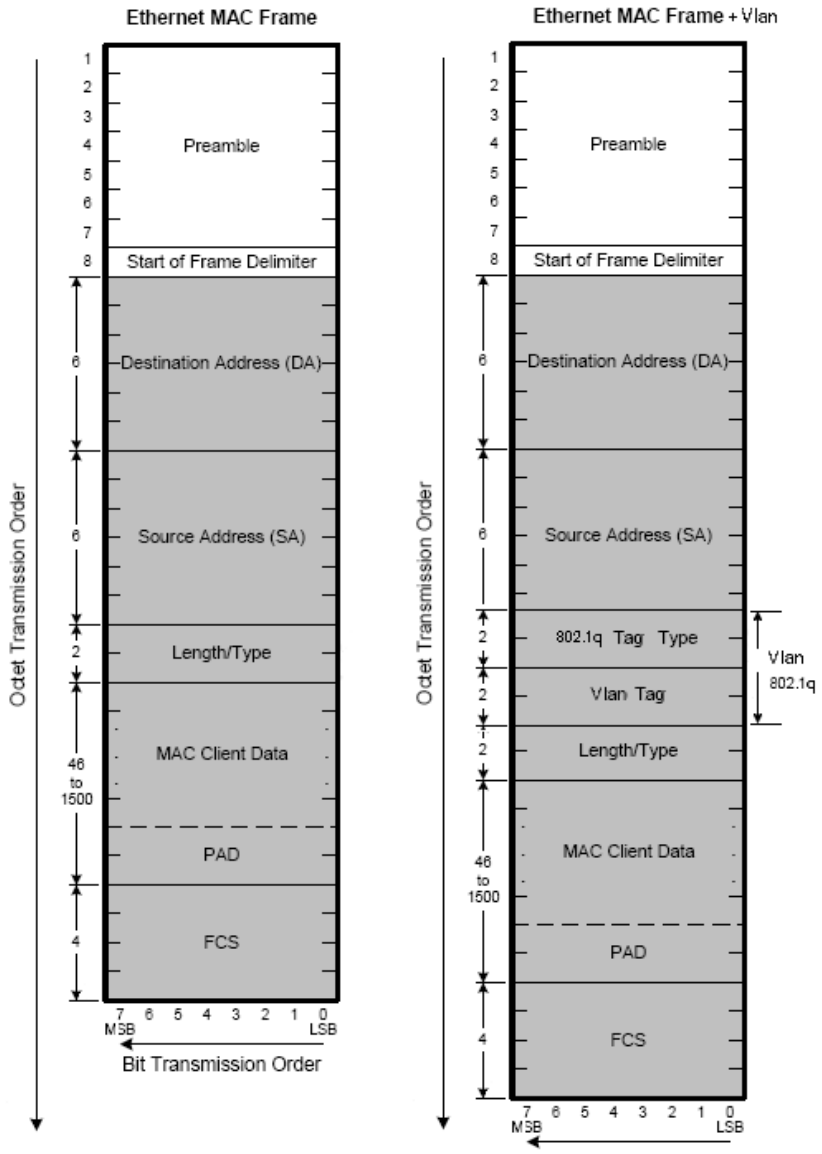


Figure 14: Types of Ethernet Frames

The PVG610A supports both frame types.

3.2.2.3 Traffic Control

PVG610A supports Class of Service (CoS) in the Rx path (i.e. packets from the Ethernet line directed to the radio). The PVG610A supports two queues (high priority and low priority). The incoming packets are directed, based on their ‘user priority level bits’ in the VLAN Tag, to the high priority queue or the low priority queue (the mapping between the 'user priority level bits' and the queues is programmable). The following table describes the VLAN TAG for VLAN Ethernet frames.

Table 1*: VLAN TAG Format*

(2 bytes)	(2 bytes)		
Type	User priority level (3 bits)	CFI (1 bit)	VLAN ID (12 bits)
0x8100	‘000’-‘111’		

Non-Vlan Ethernet frames can be directed to one of the queues according to a predefined configuration.

The low priority queue is served only when the high priority queue is empty.

The PVG610A contains 32Kbyte RAM, dedicated to the Ethernet FIFO's (including Tx and Rx FIFO's). The memory allocation for each FIFO is programmable (as long as all allocations sum up to 32kByte).

Flow control mechanisms exist across the radio link and toward the Ethernet line.

3.2.2.4 Management of Ethernet Link

The PVG610A support Ethernet PHY management via MDC/MDIO lines and according to the management protocol as defined in 802.3 standard.

3.2.2.5 Monitoring

PVG610A support RMON counters (similar to RFC 1757).

3.2.3 STM-1/OC-3 Interface Block

The STM-1/OC-3 interface block supports the connection of two STM-1/OC-3 links. The following figure illustrates a typical connection of an STM-1/OC-3 link to the PVG610A.

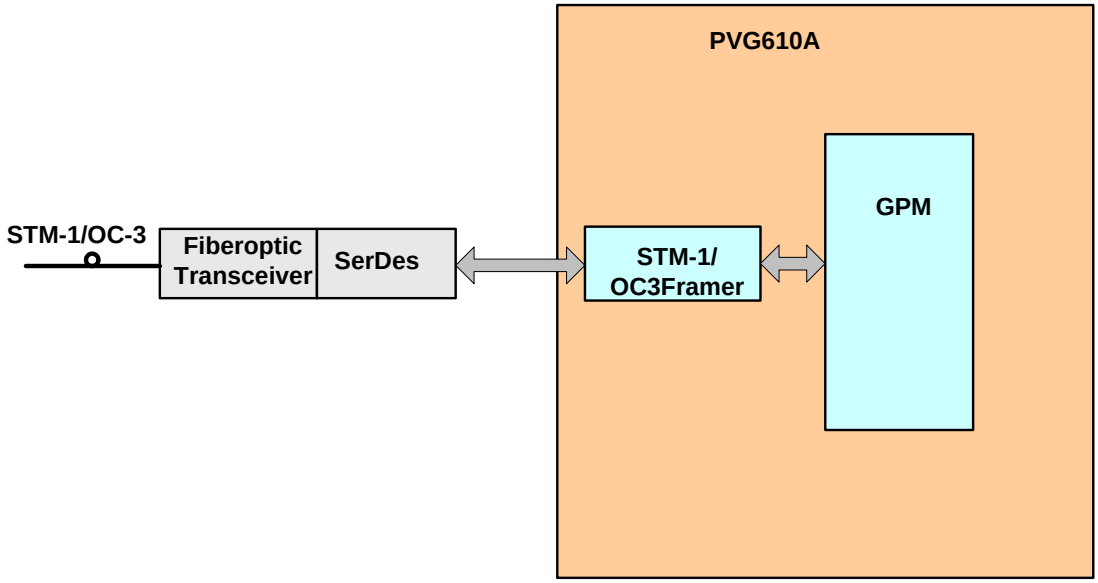


Figure 15: STM-1/OC-3 Connection to PVG610A

The fiber-optic transceiver converts the incoming optical signal to a serial digital electrical signal. It is then converted to an 8 bit parallel data by the SerDes and routed to the STM-1/OC-3 Framer in the PVG610.

The STM-1/OC-3 framer in the PVG610A supports the following features:

- Extraction/insertion of TOH/DCC bytes
- Alarms and performance monitoring
- PRBS insertion/monitoring
- External VCXO with PWM for clock extraction (in the Tx direction)
- AIS and RDI forced insertion toward line and radio direction

3.2.3.1 STM-1/OC-3 Block Diagrams

Receive Path

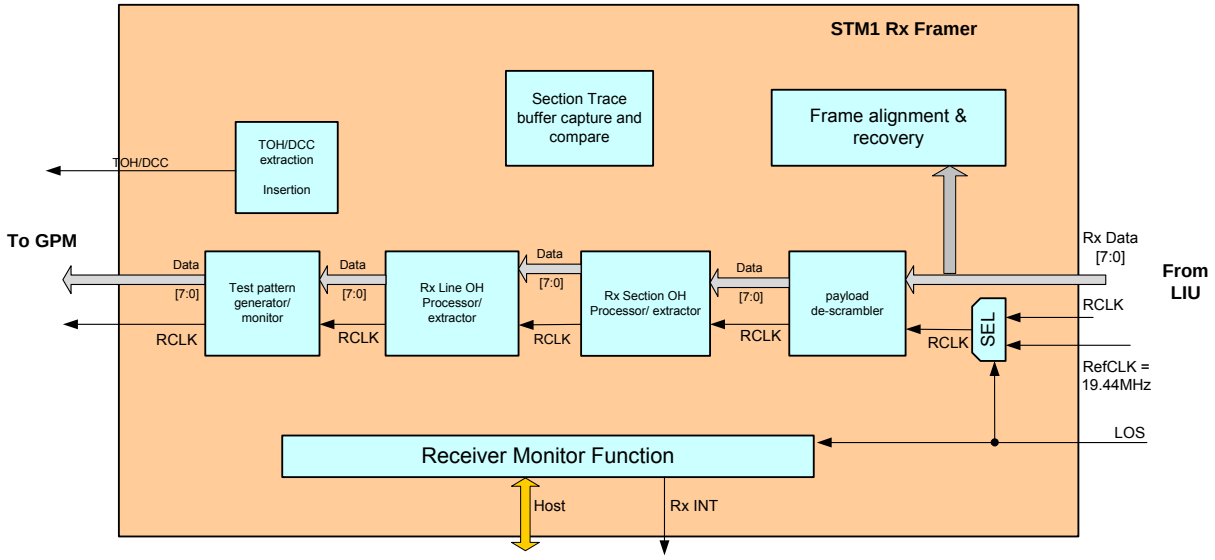


Figure 16: STM-1/OC-3 Rx Framer Block Diagram

The Receive bus of Rx Data [7:0] and clock (RCLK) from the SerDes is shown at the right side of the drawing. The data is routed to the frame alignment and recovery block in which the beginning of an STM1/OC-3 frame is searched. When alignment is reached, the data passes through the payload de-scrambler block in which a (X7+X6+1) polynomial is applied.

Following the de-scrambler block the following take place;

Monitoring of Section and Line OH alarms (LOS, LOF, AIS, RDI, and TIM)

Performance monitoring of B1, B2 and M1 counters

Extraction/insertion of TOH/DCC bytes

An option is provided to generate/monitor PRBS before bytes are sent to the GPM.

Transmit path

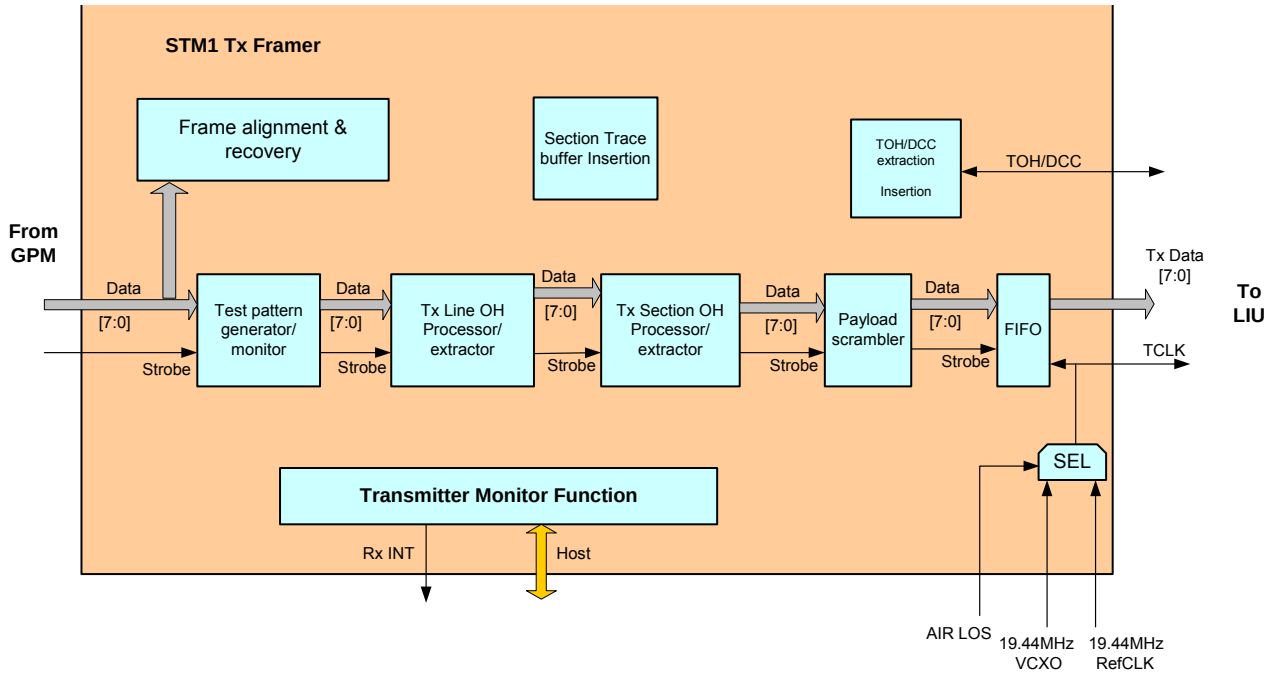


Figure 17: STM-1/OC-3 Tx Framer Block Diagram

The transmit bus of Tx Data [7:0] and clock (strobe) from the GPM is shown at the left side of the drawing. It is routed to the alignment block in which the beginning of an STM1/OC-3 frame is searched. When the alignment is completed, TOH/DCC bytes are extracted/inserted.

An option is provided to generate/monitor PRBS before the bytes are sent to the Scrambler. Scrambled data of X7+X6+1 polynomial and a reconstructed clock are sent to the SerDes through a synchronizer. The clock is built using a first/second order loop and a VCXO.

3.2.3.2 STM-1/OC-3 Frame Description

The STM-1/OC-3 data rate is 155.52 Mbps. It consists of 3 frames where each frame has 810 bytes and is generated 8000 times in a second (3 frames every 125 µsec). (155.52 Mbps = 3 x 810 bytes x 8000 x 8 bit)

Below is a diagram showing the STM-1/OC-3 frame format.

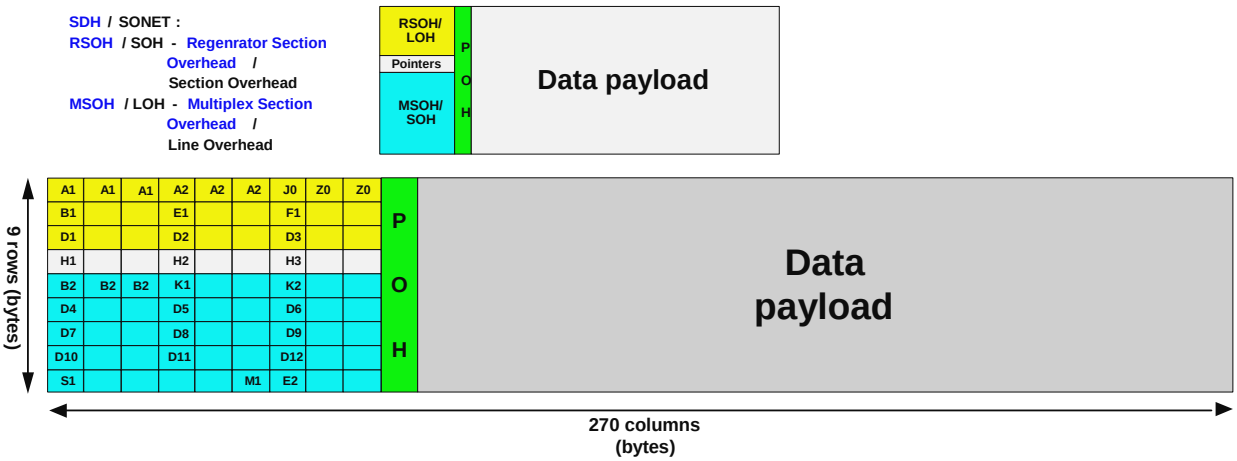


Figure 18: STM1/OC-3 Frame Format

Table 2: Transport Overhead (TOH) Bytes Description

RSOH/SOH	
Byte	**Description**
A1, A2	Indicates the beginning of the STM-1 frame (A1:'11110110', A2:'00101000'). The frame alignment word is comprised of 3 A1 bytes followed by 3 A2 bytes.
J0	Regenerator Section trace, used to transmit a section access point identifier (one byte or 16 byte string message) so that a section receiver can verify its continuous connection to the intended transmitter.
Z0	Spare, reserved for future use.
B1	Regenerator Section error monitoring. The BIP-8 is computed over all bits of the previous STM-1 frame after scrambling and is placed in the B1 byte of the current frame before scrambling.
E1	Provides order wire channels for voice communication between regenerators.
F1	Reserved for user purposes.
D1-D3	Data Communication Channels (DCC). A 192 kbit/s channel used from a central location for alarms, control, and monitoring and management functions.
MSOH/LOH	
Byte	**Description**
B2	Multiplex Section/Line error monitoring. The BIP-24 is computed over all bits of the previous STM-1 frame except for the first three rows and is placed in the B2 byte of the current frame.
K1, K2	Allocated for APS (Automatic Protection Switching) signaling. Also used to indicate MS-AIS/AIS-L and MS-RDI/RDI-L.
D4-D12	Data Communication Channels (DCC). A 576 kbit/s channel used from a central location for alarms, control, monitoring and management functions.
S1	Synchronization Status. Bits 5-8 are used to carry the synchronization messages.
M1	Used to send/detect MS-REI/REI-L, carry the count of errors detected in B2 byte.
E2	Provides order wire channel for voice communication between multiplexers.

3.2.3.3 Section/Line Overhead Extraction/Insertion

The user can configure to:

Extract all TOH bytes (5.184Mbps) and insert TOH bytes in a payload rate of 64Kbps up to 5.184Mbps (in 64Kbps granularity).

The extracted bytes can be directed to a dedicated interface or to the internal processor.

Inserted bytes can be sourced at a 64kbps granularity from the dedicated interface or from the processor.

Extract/insert Section DCC (192Kbps)

The extracted bytes can be directed to a dedicated interface or to the internal processor.

Inserted bytes can be sourced from the dedicated interface or from the processor.

Extract/insert Line DCC (576Kbps)

The extracted bytes can be directed to a dedicated interface or to the internal processor.

Inserted bytes can be sourced from the dedicated interface or from the processor.

TOH/DCC bytes can be extracted/inserted from/into the line or radio direction.

3.2.3.4 Alarms

The PVG610A identifies alarms and reports their appearance to the host via an interrupt mechanism. The following alarms are supported:

- Loss of Signal (LOS)
  - LOS from the line identified
  - AIS and RDI are injected as required by SONET/SDH standard (unless in manual control mode)
- Loss of Frame (LOF)
  - LOF from the line identified
  - AIS and RDI are injected as required by SONET/SDH standard (unless in manual control mode)
- Out of Frame (OOF)
  - OOF from the line identified
- Multiplexed Section Alarm Indication Signal (AIS) / Line Alarm Indication Signal (AIS-L)
  - MS-AIS / AIS-L from the line identified
- Multiplexed Section Remote Defect Indication (MS-RDI) / Line Remote Defect Indication (RDI-L)
  - MS-RDI / RDI-L from the line identified
- Multiplexed Section Remote Error Indication (MS-REI) / Line Remote Error Indication (REI-L)
  - MS-REI / REI-L from the line identified
- Regenerator Section Trace Identifier Mismatch (RS-TIM)
  - RS-TIM from the line identified
- Regenerator Section Trace Identifier Unstable (RS-TIU)
  - RS-TIU from the line identified

3.2.3.5 In Band EOW

While using in-band EOW, the STM-1's E1/E2 bytes (in the TOH field) are used as source/sink to the EOW PVG610A interface. It can be applied to either the Air or the optical line.

3.2.3.6 Monitoring

The following events are monitored by PVG610:

- Section BIP-8 errors (B1)
- Line BIP-24 errors (B2)
- Line REI events (M1)

The monitoring is conducted on events from the line direction.

3.2.3.7 PRBS Generation & Monitoring Description

PVG610A supports Pseudo-random bit sequence (PRBS) generation and Monitoring. It generates and monitors an unframed (2^{23} – 1) payload test sequence in an STM-1 frame. The test sequence is inserted in the SPE bytes (POH + Payload), i.e. all bytes except the TOH.

The generating polynomial is $g(x) = X^{23} + X^{18} + 1$.

3.2.4 General Purpose Interface (GPI)

The PVG610A supports a General Purpose interface (GPI). The GPI consists of a data (Bytes), clock, and control signals supporting asynchronous (using flow control) and synchronous transfer modes.

There are two options for using the GPI; with an external framer or with an internal framer (in the GPM). Each option can support ACM and can be operated in synchronous or asynchronous mode.

In using the external-framer option the GPI block is connected at the interface side to the user External Logic unit and within the PVG610A it is linked directly with the modem, bypassing the GPM.

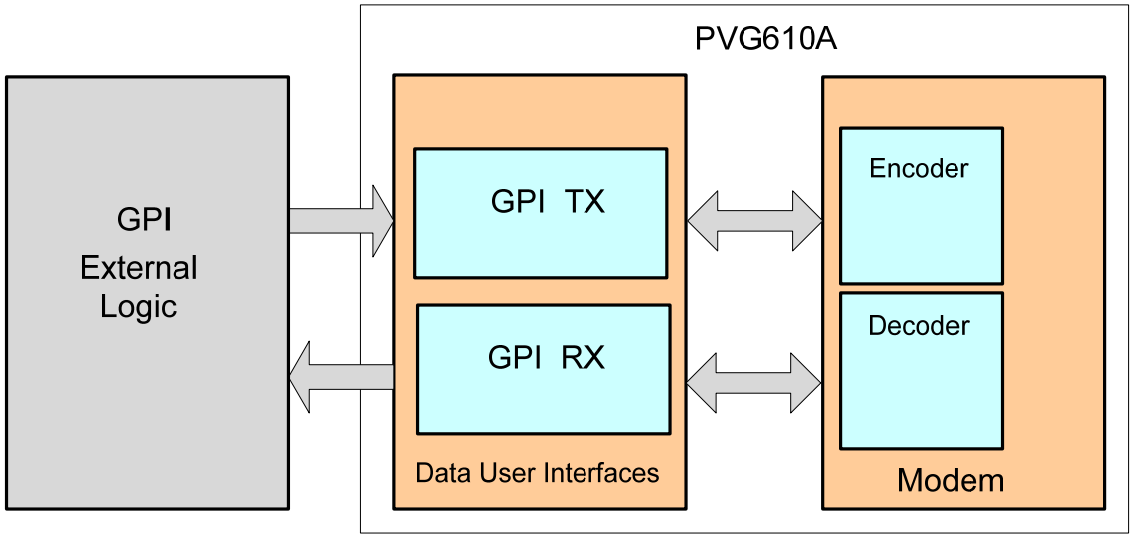


Figure 19: External Mode - GPI connecting directly to the Modem

When using the internal framer, the GPI is integrated into the PVG610A user interface block operating as one of several ports connecting to the GPM, as shown in the drawing below.

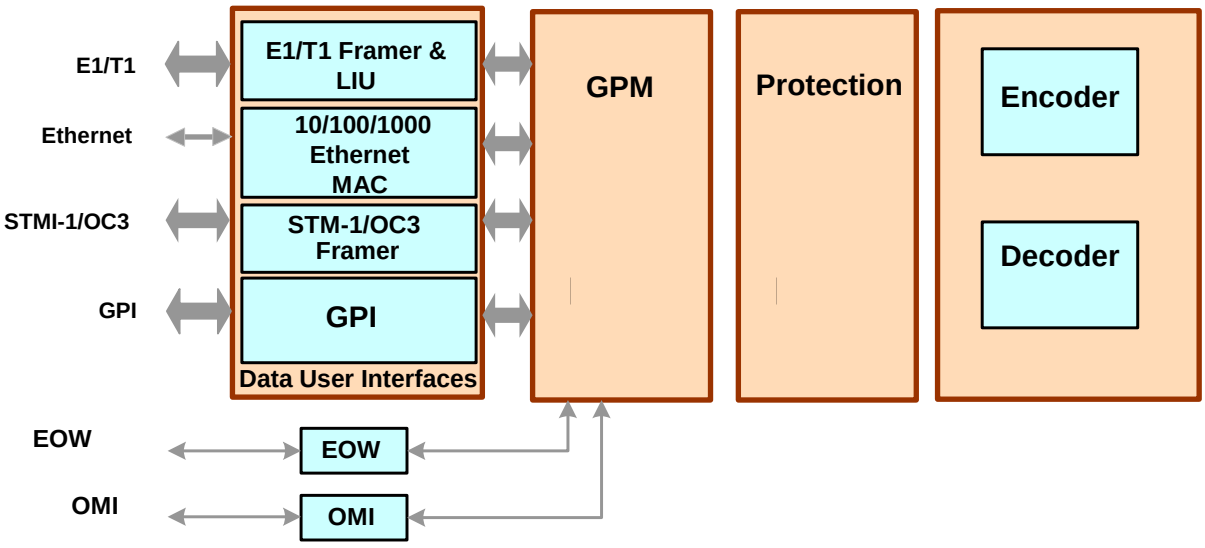


Figure 20: Internal mode, GPI Port connecting to the GPM

The GPI block includes data FIFO buffers in the transmission and reception data paths. In the transmit direction a 2kBytes FIFO buffer is used. In the receive direction a 4kBytes FIFO is used. Both FIFO buffers are available when using internal framer (GPM) or external framer.

3.2.4.1 Transmitted Symbol Timing

The PVG610A enables to lock the transmitted symbol timing on external source (see 3.6.2.1). There are two modes which support this:

1. FIFO mode: the digital PLL phase-detector is based on the number of bytes in the GPI TX data FIFO. Thus, the loop strives to maintain a constant number of bytes in the transmitter byte FIFO. This mode is relevant only for Synchronous GPI with external framer.
2. Multiplier mode: a digital PLL multiplies the incoming GPI clock signal (TX_CLK) by a rational factor of M/N to generate the internal symbol clock. The ratio N/M is twice the ratio of the symbol clock to byte clock. This mode can be used in Asynchronous GPI with external framer or when the GPM is activated.

The second order loop filter (in both modes) is programmable and can support a wide range of bandwidths. A very narrow bandwidth can be selected to improve the system jitter-tolerance and jitter-transfer characteristics. The generated symbol clock is further processed by a digital PLL that is part of the transmit-timing module. The dynamic performance of the modem clock chain is determined by the combination of the two loops.

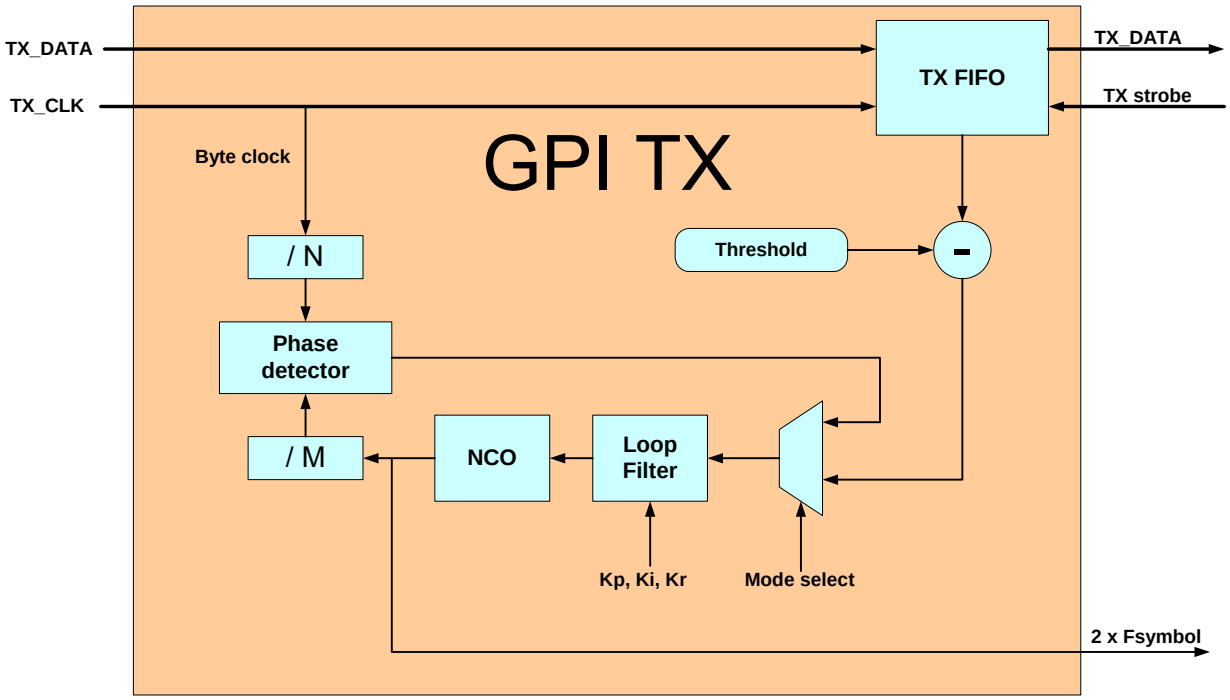


Figure 21: TX Symbol Clock Locking on External Source

3.2.4.2 Synchronous GPI

In synchronous GPI modes, data is transferred through the GPI at a constant rate (i.e. fixed number of bytes for every fixed number of TX/RX_CLK clock cycles).

When using external framer the transmitted symbol timing is locked on the data rate by using the FIFO Lock Mode as explained above.

When using the GPM, the transmitted symbol timing is free running (or locked on TX_CLK by using the Multiplier Lock mode as explained above). In this case the adaptation between the GPI traffic source rate and the modem transfer rate is done internally, between the GPI and the GPM blocks (by means of stuffing bytes in the GPM frame).

At the receive side the GPI RX Clock is reconstructed by an external Direct Digital Synthesis (DDS) block. The PVG610A supplies the DDS_CLK signal and DDS [7:0] data to enable the clock construction. The DDS port outputs samples from a sine wave look up table. The DDS clock has to be at least four times the desired synthesized clock frequency.

A digital PLL is used for setting the synthesized clock frequency. The PLL's phase detector is based on the number of bytes in the data FIFO. Thus, the loop strives to maintain constant number of bytes in the receiver byte FIFO. A second order programmable loop filter is used and can support a wide range of bandwidths. A Very narrow bandwidth can be selected to improve the system jitter-generation and jitter-transfer characteristics. The jitter performance of the generated byte clock depends not only on this module but also on the receiver timing recovery module.

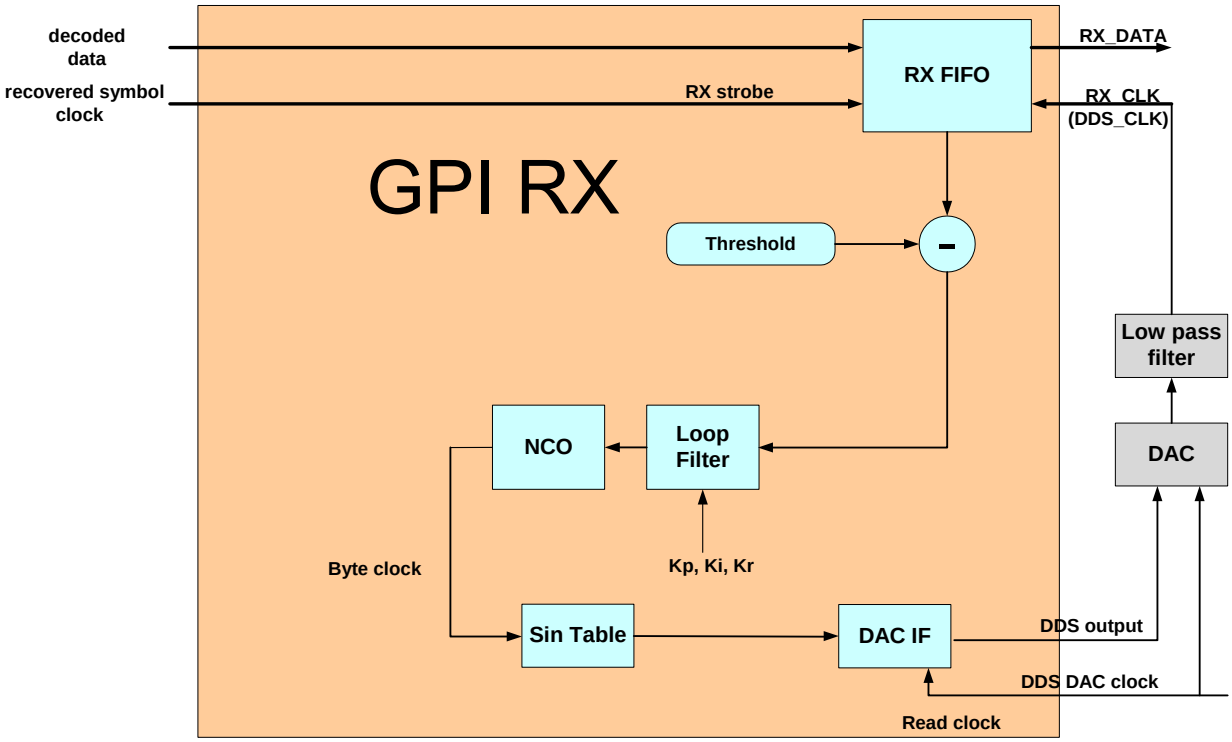


Figure 22: Synchronous GPI – RX Clock Reconstruction

3.2.4.3 Asynchronous GPI

In asynchronous GPI mode the GPI clock is not synchronized to the data. The only requirement for Tx_CLK and RX_CLK is that their frequencies are higher than the highest byte transfer rate.

In asynchronous GPI mode, the transmitted symbol timing is free running (or locked on TX_CLK by using the Multiplier Lock mode as explained above). The adaptation between the GPI traffic source/sink rate and the modem transfer rate is done with FIFO's in the GPI RX/TX ports and GPI flow control signals.

3.2.4.4 PRBS Generation & Monitoring

PVG610A supports Pseudo-random bit sequence (PRBS) generation and Monitoring for the GPI. It generates and monitors an unframed (215 – 1) payload test sequence.

3.3 General Purpose Multiplexer (GPM)

In the transmit direction the General Purpose Multiplexer (GPM) organizes data from multiple sources, builds data frames to be transmitted and sends frames toward the modem. In the receive direction, the GPM extracts the different data types from the GPM frame and distributes the data to the addressed user interfaces

3.3.1 GPM Block Description

The General Purpose Multiplexer (GPM) is comprised of 28 input tributaries and 28 output tributaries. Each tributary may be enabled or disabled depending on the GPM initial programmed configuration. Each tributary carries a specific service (i.e., E1/T1, STM1, etc.). The total number of enabled tributaries determines the size of the GPM frame header.

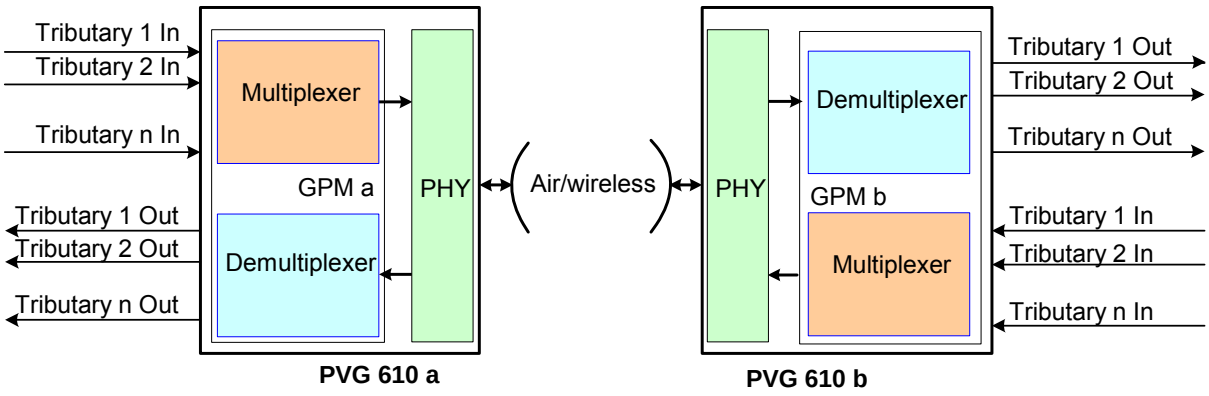


Figure 23: GPM Functioning Diagram

There are 28 Tributaries as listed in the following table:

Table 3: List of Tributaries

Tributary Number	Type
1	GPI
2	Ethernet
3	STM-1/OC-3
4	STM-1/OC-3
5	EOW
6	OMI
7-27	E1/T1/J1
28	IMB

In the GPM (Transmit and Receive), there is a byte spreading algorithm that evaluates each tributary according to its configured bandwidth. Each tributary is allocated a certain number of bytes in each transmitted Airframe. The algorithm distributes the bytes in a way that prevents FIFOs overflow or underflow. Each ACM profile has a predefined configuration known to the GPM. There are up to 16 ACM profiles. As the ACM is changed, the GPM starts a new Airframe with the relevant bytes allocation for the tributaries.

3.3.2 Rate Adaptation

When a synchronous tributary doesn't have enough data to fill the pre-allocated data field, up to 16 dummy bytes (Justification bytes) are stuffed instead. These bytes are removed in the receiver and are transparent to the user. The user configures the maximum justification bytes per frame per tributary in the configuration file.

For asynchronous interfaces (Ethernet or Asynchronous GPI) the stuffing mechanism is turned off. The Ethernet block in the PVG610A is delivering GFP idle bytes to the GPM if there is no Ethernet data ready for transmission. In Asynchronous GPI it is the responsibility of the user to add idle bytes (by using GFP or similar protocol) and make sure that the GPI fifo in the PVG610A doesn't get empty.

3.3.3 GPM Frame

The GPM generates one GPM Frame for each airframe. The GPM frame is constructed of the following fields:

The GPM frame contains the following fields:

- Sync Byte: 1 Byte. Used to point the start of GPM frame.
- ACM field: 1 Byte. Specifies which of the 16 profile is in use. This byte is protected in (4,7) Hamming code. This byte is removed if ACM is not in use.
- JCB field (Justification Control Byte): N bytes (N being the number of synchronous tributaries in the frame). The JCB indicates the number of justification bytes (dummy bytes) that are added to the GPM frame for the specific tributary in the specific frame. The JCB is protected with one of the following codes:
    - (4,7) Hamming code: supports up to 16 justification bytes per frame
    - 8 repetition code: supports one justification byte per frame (provides better immunity against noisy channels)
- Payload field: all tributaries are multiplexed in this data field.

3.3.4 3.3.4 OMI

The OMI is used to transfer information between the host of the local PVG610A station to a remote PVG610A station. The OMI information is embedded in a selected field within the transmitted frame.

The OMI is glue less to generic CPU serial communication interface (such as Motorola SCC).

3.3.5 Out of Band EOW

While using Out-of-Band EOW, a 64 kHz or 128 kHz channel is allocated in the GPM frame for EOW. The EOW data from the EOW channel is mapped into the EOW interface

3.4 Protection Block

The PVG610A supports a variety of protection modes to confront with transmission failures. Four protection modes are listed below.

Frequency diversity – a backup channel that transmits in a different frequency

Space diversity – a single transmitter that transmit the same carrier to two receivers located in different sites

Hot Standby – similar to space diversity except that the transmitted data is also transferred to the backup system to support accelerated switchover

1:N protection – a single channel can be used as a protection channel for N channels.

The protection procedures are based on standby protection boards operating in a redundancy mode and a built in protection block in the PVG610. In case of a transmission failure the traffic is routed to the protection transmitter board. In case of a receive failure in the main PVG610A board the traffic is routed to a protection receiver board.

The routing of traffic is controlled by a built in protection block in the PVG610A chip.

Below is a drawing of a PVG610A based system in which the unit at the left is in a transmit mode and the other one is in a receive mode.

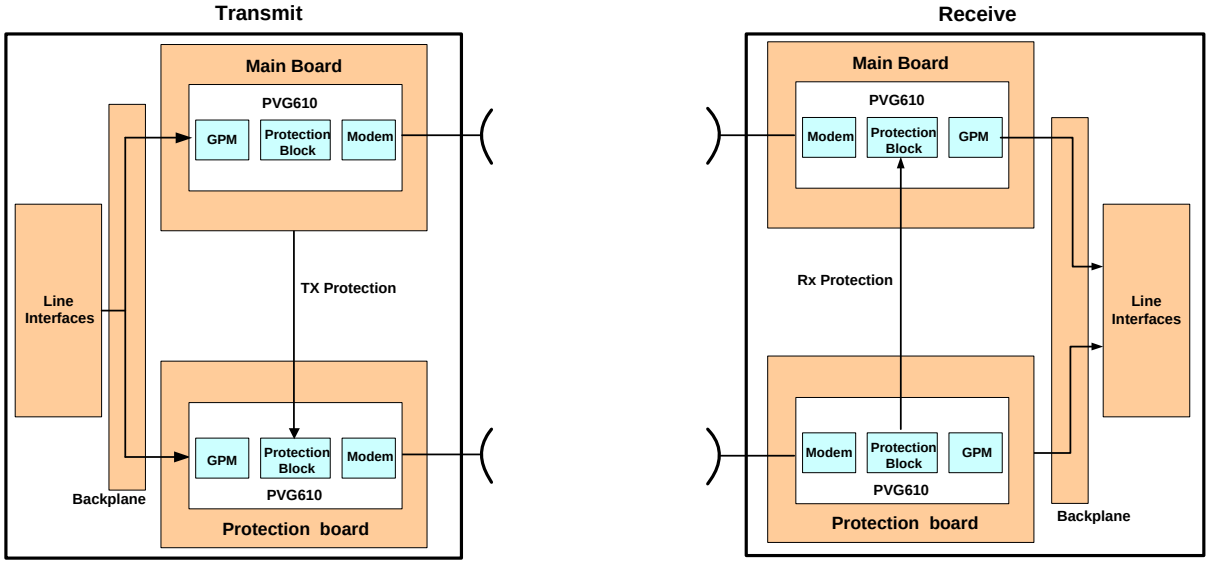


Figure 24: Operating in a protection mode

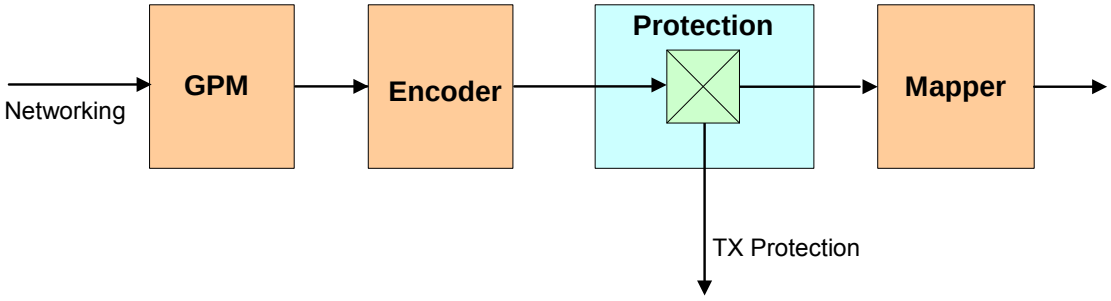
At the transmit end, the protection block in the main PVG610A distributes the data to the modem in the main board and to the protection PVG610A board through the Tx Protection port. The data can be continuously transmitted to the receive unit according to a selected protection mode of operation listed above.

At the receive end, both main and protection PVG610A boards receive the signal. The data is then demodulated and decoded.

The PVG610A at the receive protection board sends the data to the main PVG610A board through the Rx Protection port. The main PVG610A has to decide whether to accept the data from the transmit board or from the receive protection board. The data is handled at an LDPC or RS block level. Upon an error in one these two data channels the PVG610A selects the other. The default path is the data channel in the main board.

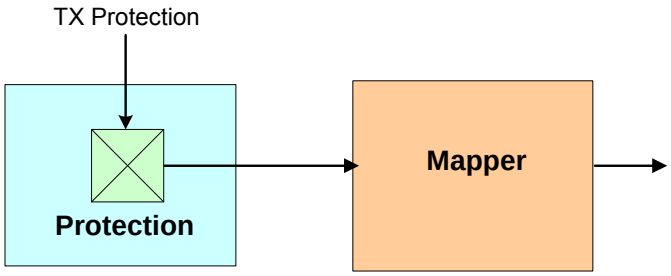
3.4.1 Transmit End

Transmit unit Main board:



Data is passed through the FEC encoder and goes on to the protection block. From the protection block data is duplicated and goes to the mapper and to the Protection board via the Tx protection channel.

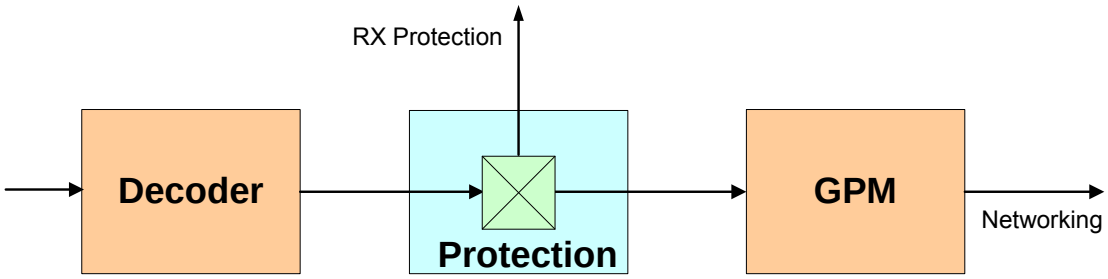
Transmit Unit Protected board:



The Tx protection channel data is received at the Protection block and passed on to the mapper.

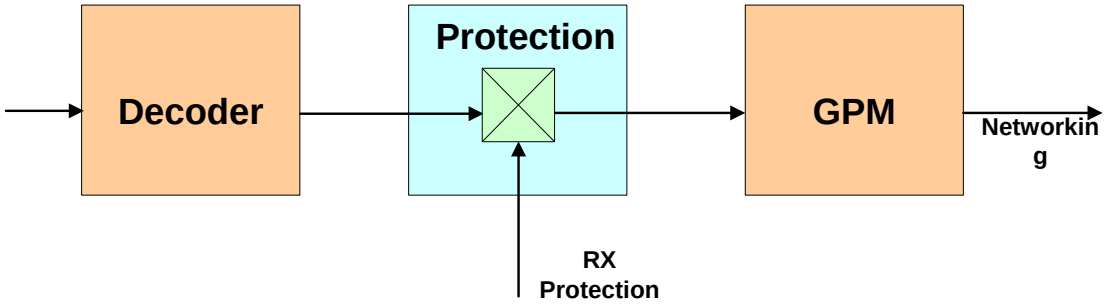
3.4.2 Receive End

Receive Unit Protection board:



Data from the decoder is distributed to the main PVG610A board through the Rx protection port and to the GPM toward the networking.

Receive Unit Main board:



Data from the decoder is sent to the matrix byte alignment circuit in the protection block while data is received at the RX protection port. The matrix byte alignment circuit in the protection block has two functions:

It makes the required alignment between RS/LDPC blocks received at the matrix byte alignment block

Per block, it selects the block to be transferred to the GPM. By defaults RS/LDPC blocks from the decoder are transferred to the GPM. In a case of a data error the matrix byte alignment transfer the block from the RX protection channel unless that also has an error.

In case of link failure in the protection channels or a HW failure in the protection board, no hit is declared i.e. data is not lost.

In case of HW failure in one of the main boards a switch over occurs to the protection board generating a failure of less than 50msec.

The Protection Block provides the following features:

- Hitless protection for 1+1 protection modes (frequency and space diversity) upon link failures.
- Enable flexible configuration of Tx/Rx Main/Protection in the same chip (SW control)
- Manual switch over support (SW control)
- AIR LOS/ALM output pin and early warnings for 1:n schemes

3.5 Cable interface Block

The cable interface block is used when the air modem is located at an outdoor unit. An analog signal between the PVG610A in the Indoor unit (IDU) and the outdoor unit (ODU) is carried over a coax cable. ThePVG610A modem in this configuration is based on Reed-Solomon FEC and designed to operate with a coax cable connecting the IDU with the ODU.

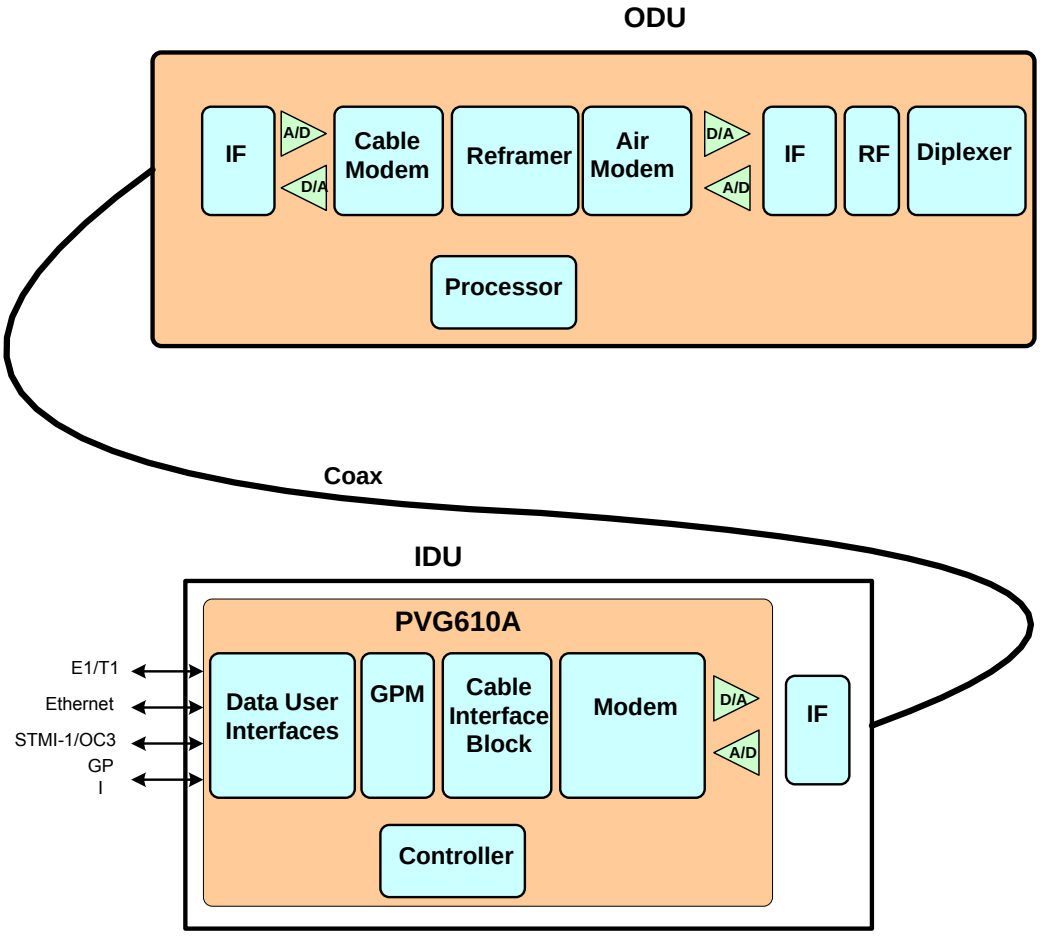


Figure 25: PVG610A supporting air modem in ODU

The cable interface block support the following features

- Enables connection between the IDU and ODU.
- Converts PVG610A GPM frames to/from Reed Solomon (RS) blocks to enable transmission in the coax cable.
- Can work with configurable RS (n,k) blocks.
- Can work with RS PHY in maximal rate of QAM256, 49.5MSPS
- Glue-less to ACM and TDD actions

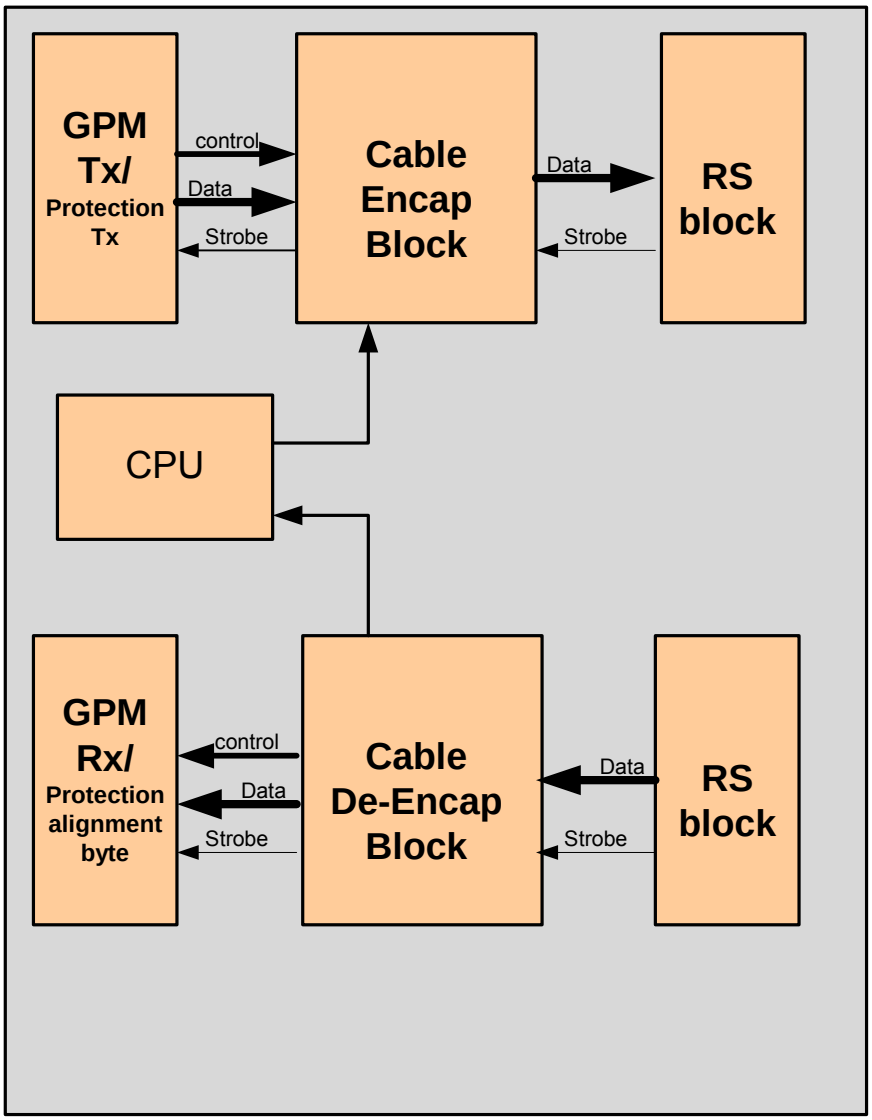


Figure 26: Cable Interface Block

The PVG610A cable encapsulation block translates signals from the GPM/GPI/Protection block to CI frames, which 'ride' over pre-defined RS blocks.

The PVG610A de-encapsulation block translates CI frame, which 'rides' over RS blocks to signals going to the GPM/GPI/Protection block.

3.6 Modem and AFE Block Description

The Encoder and Modulator at the modem transmit blocks create the transmitted airframe from data received from the GPM.

The encoder adds LDPC or Reed Solomon encoding bits in creating the Forward Error Correction (FEC). The bits are then mapped into symbols according to the selected modulation. The symbols are then modulated into (I) and (Q) signals or into an IF signal.

The digital format of the airframe is converted to analog signals by the Analog Front End (AFE) and sent for transmission.

At the receive direction the AFE converts the received analog signal to digital format and sends it to the demodulator block. The digital bits are stripped by the demodulator and sent to the decoder for error correction.

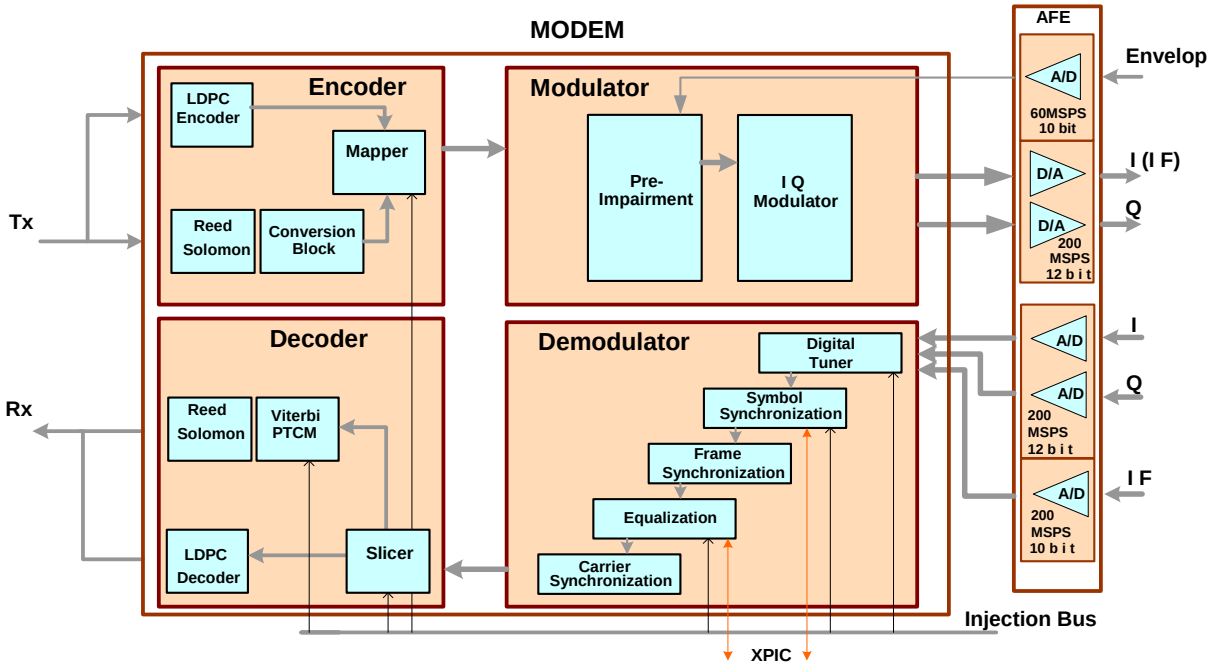


Figure 27: Modem and AFE Block Diagram

3.6.1 Encoder Block Description

The Encoder Block contains the following sub-blocks:

- Low Density Parity Check (LDPC) encoder
- Reed Solomon encode
- Conversion Block
- Mapper

3.6.1.1 LDPC Encoder Description

The LDPC encoder architecture is based on the lower triangular matrix shape of the parity columns. The encoder's architecture is serial, thus some latency is introduced to the output. The encoder is programmable, supporting various code lengths and rates on the same hardware.

The LDPC code is based on permutation block matrices. For a code rate of R and a codeword length of n bits, with k = R n information bits and m = (1 – R) n parity bits, there is a parity check matrix H of size m x n. This parity check matrix is constructed of block matrices of size (Z x Z). Each such block matrix is either a zero matrix or a permutation of the identity matrix.

Low-density parity check (LDPC) code is a special case of linear error correcting block code. This code's parity check matrix, H, is highly sparse, enabling a small amount of storage in memory. Each codeword satisfies H c = 0, where c is a codeword of length n. The matrix H is of size (m x n), where (m = n – k) is the number of redundant bits added to information bits. Theoretically, since a systematic encoding is desired, one has to find the generating matrix, G, which spans an orthogonal space to the one spanned by H, i.e.

(G ·HT = 0). To generate the desired systematic property, the matrix G has to be ranked by performing linear row combinations such that: G = [I | P]. Since the LDPC matrix's size is extremely large, finding the orthogonal matrix to H is not a feasible task. Encoding is done directly from the parity check matrix H.

3.6.1.1.1 Encoding Algorithm

By enforcing a structure on the parity check matrix, H, a linear complexity encoding can be achieved. The constructed code is systematic such that the first Kb = K/Z block columns contain information bits and the last Mb = M/Z block columns contain parity check bits. The last Mb block columns of H forms an almost block lower triangular matrix.

3.6.1.1.2 LDPC Mother Rates

The supported mother code rates by the LDPC code are:

R = ½ and R = ¾.

Puncturing either one of these code rates will attain higher codes rates.

3.6.1.1.3 LDPC Code Puncturing

The LDPC code supports various code rates with fine granularity. These rates are obtained by puncturing the codeword at the encoder output by np bits. The punctured code is based on puncturing either a mother code of rate ¾ or a mother code of rate of ½.

3.6.1.1.4 LDPC Levels of Coding

The LDPC supports two ways of encoding. One is a non-multiple coding and the other is a multiple coding. The first is used for low modulations of up to 32 QAM and the other is used for high modulation 64 QAM, 128 QAM, and 256 QAM.

Non-multiple coding: Low constellations are fully LDPC encoded, i.e. all transmitted bits are LDPC encoded and mapped to symbols. The LDPC Encoding in a non-multi-leveling mode is shown below.

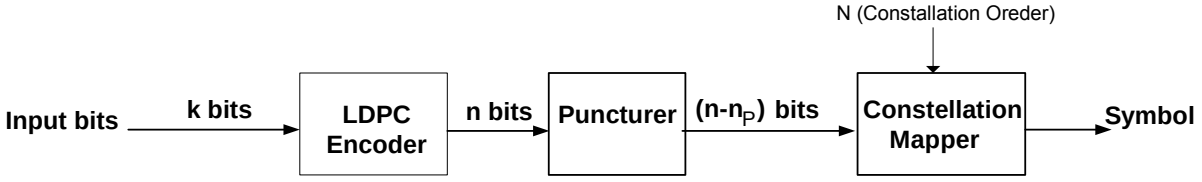


Figure 28: LDPC Non-Multi Level Coding

A block of k information bits is encoded to an LDPC codeword of n bits. Next, this LDPC codeword is punctured in np bits. The remaining n - np bits are divided into groups of log2N bits (where N is the number of symbols in the constellation) and each group is mapped to a symbol. The np ensures that (n - np) / (log2N) is an integer.

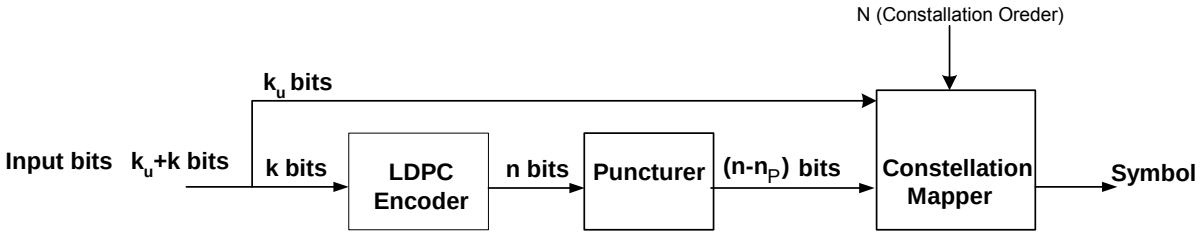


Figure 29: LDPC Multi-Level Encoding

Multi-Level Coding: For high constellation orders, (64,128,256), only four bits are encoded and the rest of log2N-4 bits are left un-coded. This constitutes one symbol.

3.6.1.1.5 Number of symbols per LDPC block

The number of symbols per LDPC block, as shown in the following tables, is derived from the modulation type, LDPC block size and the puncturing rate.

Table 4: Number of symbols per LDPC block

Modulation	Block Size			
	2016	4032	8064	16128
QPSK	1008	2016	4032	8064
16QAM	504	1008	2016	4032
32QAM	396 (1)	804 (2)	1608 (3)	3212 (4)

(1) Due to minimal number of punctured bits = 36

(2) Due to minimal number of punctured bits = 12

(3) Due to minimal number of punctured bits = 24

(4) Due to minimal number of punctured bits = 48

Table 5: Number of symbols per LDPC block (Multi level)

Modulation	Block Size			
	2016	4032	8064	16128
64QAM (1)	504	1008	2016	4032
128QAM (2)	504	1008	2016	4032
256QAM (3)	504	1008	2016	4032

(1) Nsym = (Nbit + 2*Nbit/4) / 6

(2) Nsym = (Nbit + 3*Nbit/4) / 7

(3) Nsym = (Nbit + 4*Nbit/4) / 8

3.6.1.2 Reed Solomon Encoder Description

The Reed-Solomon encoder is a programmable encoder with a block length of K = 6 to 255. The number of check bytes can be set from 0 to 32, corresponding to T = 0 to 16 byte correction capability.

The code generator and field polynomials are:

Generator polynomial:

$g(x) = (x + \alpha 0)(x + \alpha 1) \ldots (x + \alpha 31)$

Field polynomial:

$p(x) = x8 + x4 + x3 + x2 + 1$

The encoder and decoder are configured independently.

3.6.1.2.1 Interleaver

The interleaver is used only with Reed Solomon coder. It re-orders data bytes so that long bursts of errors are distributed among several Reed-Solomon codewords and thus have a better chance of being corrected. When operating with concatenated codes, the interleaver is essential to compensate for the error multiplication effect of convolution inner codes.

The interleaver (and de-interleaver) is a Forney type convolutional function with programmable depth (B) and length (M), allowing it to accommodate any Reed-Solomon block size (i.e. M*B = N, the RS codeword length). The sync byte is used to synchronize the interleaver.

The interleaver depth (or number of branches) may be set from 2 to 12. An interleaver with depth B distributes sequential data into B different Reed-Solomon codewords. The depth is selected so that typical length error bursts can be properly distributed.

The maximum branch, M, may be set at any length as long as the required memory does not exceed 1386 bytes.

The interleaver delay can control the latency of the modem. The combined transmit and receive interleaver delay is: Interleaver Delay (in bytes) = M*B*(B-1).

3.6.1.3 Convolutional PTCM

The convolutional encoder arithmetically combines 7 sequential data bits to create two output bits (X,Y) for each input. This process introduces “history” or memory to the data stream so that the decoder can decode data corrupted by noise using knowledge of previously decoded data.

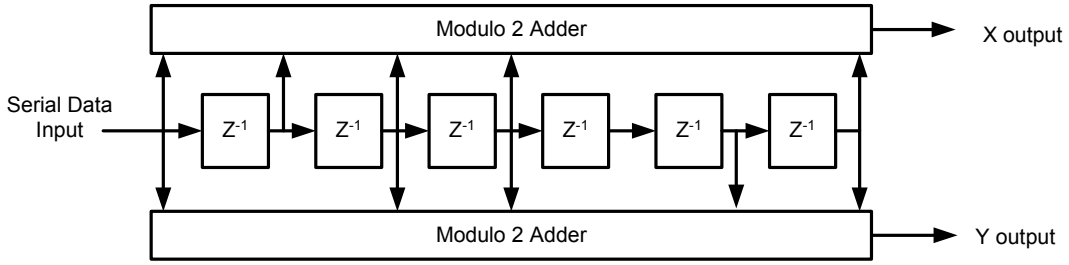


Figure 30: Convolutional PTCM Block Diagram

The puncturing machine operates on bit-pairs output from the convolutional encoder. It selectively deletes some bits. At the receiver end, the deleted bits are re-inserted with a null before decoding. This degrades the performance of the convolution-coding scheme in exchange for reduced overhead.

QPSK and 16 QAM modulations can be used in a pure convolutional mode, where the encoder and puncturing machine processes all user data.

The following table illustrates the puncturing pattern used for different rates.

Table 6: Net Convolution Puncture Rate

NET CONVOLUTION + PUNCTURE RATE				
1/2 (no action)	2/3	3/4	5/6	7/8
X: 1	X: 1 0	X: 1 0 1	X: 1 0 1 0 1	X: 1 0 0 0 1 0 1
Y: 1	Y: 1 1	Y: 1 1 0	Y: 1 1 0 1 0	Y: 1 1 1 1 0 1 0
1 = Transmitted bit; 0 = Deleted bit				

Punctured convolution coding is available for QPSK and 16QAM operation. The following table presents available modes.

Table 7: Convolutional Code Puncture Rates

MODULATION	PUNCTURE RATE
QPSK	1, 1/2, 2/3, 3/4, 5/6, 7/8
16QAM	3/4, 7/8

3.6.1.4 Mapper Description

The Mapper module takes coded bits and maps the bit stream into symbols. The module is highly programmable to support different constellations. The mapper is completely programmable and supports modulations up to 256QAM.

The Mapper supports three standard gray mapped constellations: Quadrature Phase-Shift Keying (QPSK), 16QAM, and 64QAM. Apart from the QPSK constellation that may be optimally combined with the convolution code, these gray mapped constellations are designed for use with no inner code (i.e. only RS code or a completely un-coded system is tested). For Trellis coded modulation or LDPC, where set-partitioning mapping is required, the mapper supports user-defined constellations. Constellations are defined on an integer grid spanning the range [-31, 32] for I and Q.

QAM types are limited to 256, 128, 64 constellations. Other constellations are completely flexible with the constellation's shape.

3.6.2 Modulator Description

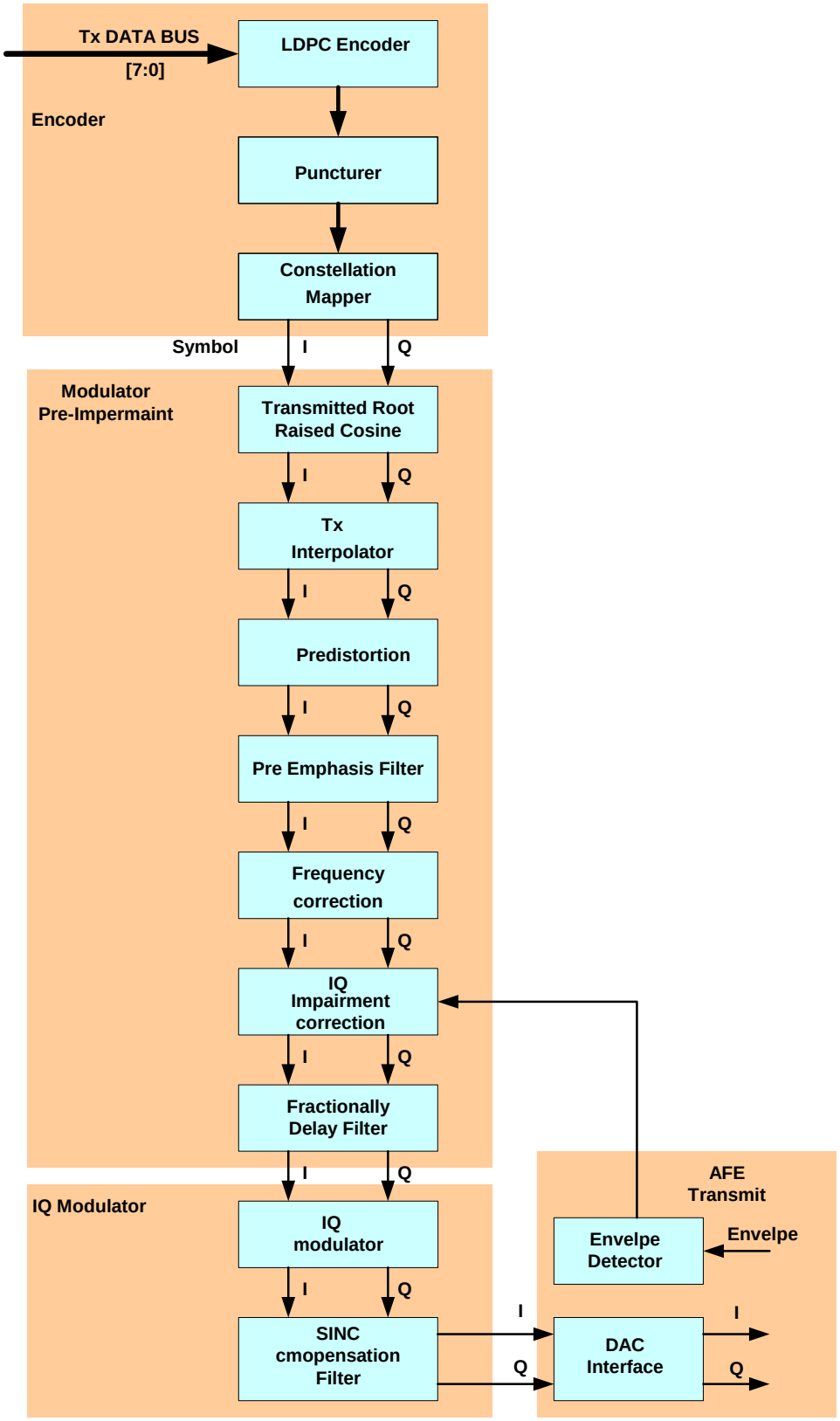


Figure 31: Modulator Block Diagram

3.6.2.1 Pre-Impairments Description

3.6.2.1.1 TRRC

The Transmitter Root Raised Cosine (TRRC) filter is an interpolating 65-tap symmetric Finite Impulse Response (FIR). It is used to shape the modulated signal spectrum. Inputs to the filter are symbols provided at the baud rate. Outputs are sampled at twice the symbol rate.

3.6.2.1.2 Tx Interpolator

The interpolator is a 10-tap filter with 1024 different sets of coefficients. Each set provides the interpolation coefficients for a different time offset, from zero to 1/2 of a symbol interval (with 1/2048 symbol accuracy). The interpolator module adjusts the rate between the sampling clock of the DAC and (twice) the symbol clock. More precisely, the module interpolates between samples from the TRRC filter (at a rate of twice the symbol rate) to generate samples at the sampling rate (Fsample).

The interpolator has two operating modes:

- **Internal mode**, where the interpolation ratio, R, is set manually and is constant; thus, the symbol rate is determined by the interpolator and locked to the DAC sampling rate.
- **External Byte Clock mode**, where the interpolation ratio is adaptive. The symbol clock generation module (TX_SYM_CLK) generates a symbol clock that is locked to the byte clock. A digital PLL adapts the interpolation ratio to maintain the selected symbol clock.

The interpolation ratio is selected so that the symbol rate is less than Fsystem / 4, where the Fsystem is the clock rate of the chip.

3.6.2.1.3 Pre-Distortion

Nonlinear pre-distortion is designed to compensate for the power amplifier's non-linearity. Successful pre-distortion reduces the required amplifier back-off, and thus increases its transmit power and amplifier efficiency. The module implements a 5th order complex polynomial to compensate for 3rd and 5th order inter-modulation. The user has to update the coefficients of the polynomial according to the transmission power. These coefficients may be evaluated by the user in two ways:

Manufacturing – the parameters are evaluated based on performance testing conducted during the manufacturing process. The parameters are constant.

Close loop – the parameters are constantly updated on the fly at the transmitter side, based on readings from the remote receiver.

3.6.2.1.4 Pre Emphasis Filter (PEF)

The pre-emphasis filter can be used to compensate for a dispersion caused in long cable runs and other IFR chain impairments. Thus the user has to design the coefficients to compensate for any linear distortion in the path between the digital nonlinear pre-distortion module and the power amplifier.

The pre-emphasis filter is a 10-tap complex coefficients filter operating at full speed (up to 200 Million samples/sec) and placed following the nonlinear pre-distortion module. The filter can be bypassed if not required. The filter is implemented as a non-symmetric, complex filter.

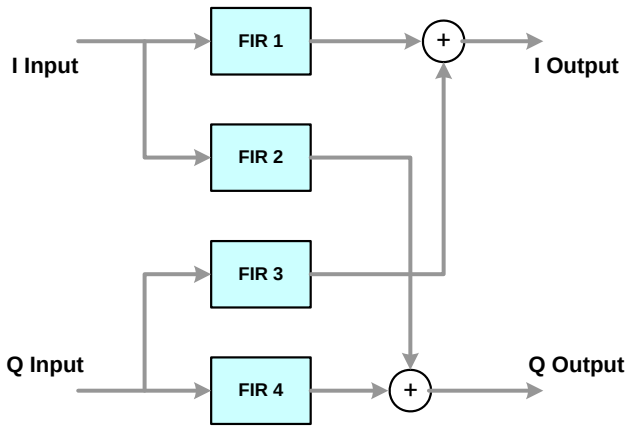


Figure 32: Pre-emphasis Filter

All coefficients are 10-bits wide with <10,8> format. A 3-bits shifter that changes the range between <10,7> to <10,14> follows each coefficient. The shifters of coefficient k in FIR1 and FIR4 are equal to each other as well as the sifters of FIR2 and FIR3. Other two 4-bits shifters are used at I and Q outputs.

The format <x, y> represents binary numbers over the range:

$\left\{\frac{\left(-2^{x-1}\right)\leftrightarrow\left(2^{x-1}-1\right)}{2^{y}}\right\}$, for <10,8> it equals: $\left\{\frac{-512}{256}\leftrightarrow\frac{511}{256}\right\}=-2\leftrightarrow1\frac{255}{256}$

3.6.2.1.5 Tx Frequency Correction

The frequency correction module is used to shift the receiver carrier frequency by a moderate amount. The frequency driving the Number Control Oscillator (NCO) is programmable within a range of ±Fsample, which allows a modulated carrier to be shifted by Fsamp/2-Fbaud/2(1+rolloff) for IQ mode

and Fsamp/4-Fbaud/2(1+rolloff) for IF mode.

Since mixing the input signal may result in an overflow, an output scalar can be used to prevent saturation. This feature is normally not used with the nominal transmitter signal levels.

3.6.2.1.6 I/Q Impairments Correction (Tx of Tx)

The Tx IQ correction module, which is placed before the digital FDF and after the Tx Frequency correction, corrects the IQ imbalances of a transmitter IQ modulator. The algorithm used in this module uses the feedback returning from the envelope detector. The correction performed by this module is controlled by an adaptive algorithm, which estimates the IQ gain and phase imbalances. In addition, it estimates and corrects the DC offset.

The Tx IQ-Correction module is designed to compensate for Tx IQ impairments generated by the analog Tx IQ modulator (and is therefore referred to as “Tx of Tx”). It comprises of several sub-modules that are all related to IQ modulation and imbalances correction due to imperfect modulation. The impairments are: IQ phase imbalance, IQ gain imbalance, and DC Offset. This module operates at the DAC sampling.

3.6.2.1.7 Fractionally Delay Filter (FDF)

The FDF is a real filter with 14 taps FIR filter, placed on the Q rail enabling adding a delay of a fraction of an integer. The I rail can be delayed by an integer number of symbols.

The FDF operates as follows:

When using direct IF synthesis (i.e., the internal Inphase Quadrature (IQ) modulator is enabled), it ensures an offset of half a sample between I and Q samples.

When using baseband modulation, it can compensate for any delay between I and Q rails up to ±7 samples.

3.6.2.2 IQ Modulator

Quadrature modulation is performed internally by a digital function (direct IF) or externally via an analog quadrature mixer (baseband). The DAC interface may be configured to support a single data stream (direct IF) or parallel I and Q (baseband) streams.

When direct IF synthesis is selected, the transmitter outputs a signal in IF frequency. The exact IF frequency is a function of the sampling rate. The fundamental Tx IF frequency is ¼ of the DAC sampling rate (FTX_SAMP). FTX_SAMP must be greater than or equal to 4 x baud rate.

Higher frequency aliased images of the fundamental IF may also be used. Aliased images appear at N x FTX_SAMP /4 where N is an odd integer. The image at ¾ FTX_SAMP is highly distorted by the SINC effect of the DAC sample and hold. This distortion may be corrected by the modem SINC compensation filter. Images at 5/4, 7/4 and 9/4 FTX_SAMP are attenuated, thus increasing the relative noise floor, but are less distorted than the ¾ FTX_SAMP image.

Recall that the exact IF frequency may be changed by the Tx Frequency Correction filter.

3.6.2.3 SINC Compensation Filter

The transmitter's digital to analog (DAC) conversion introduces frequency distortion due to the use of sample and hold circuits. Assuming perfect zero-order-hold implementation, the DAC has a sinc-shaped frequency response.

Given the bandwidth of the transmitted signal and the practical sampling rates, this non-flat frequency response requires a compensation filter to maximize the system's performance. The SINC filter can be used to correct for DAC distortions when generating baseband outputs or when synthesizing IF. The selected IF frequency and sample rate determine the appropriate set of coefficients. The SINC module implements a 15-tap symmetric FIR. Coefficients are programmable to support the different modes of operation (IF, baseband). Programmability also provides an opportunity for optimizing the compensation for a specific DAC used in the system (assuming its response is not exactly sin(x)/x).

3.6.3 Analog Front End (AFE) Description

The AFE has DAC and ADC devices providing a digital/analog and analog to digital interface between the PVG610A and the analog circuits. Several converters options are available so that baseband and direct IF sampling can be used.

A digital loopback mode is available at the digital side of the DAC/ADC units. When the user activates the digital loopback mode (via API or configuration file) the digital signal arriving to the DAC is connected to the ADC output (toward the receive path of the device).

An additional ADC is included for the envelope detector functionality. The ADC output is connected directly to the Tx IQ correction block. Also, the PVG610A has the option to be connected to an external ADC and DAC. Accordingly, there are two AFE digital interfaces available in the PVG610A pin out. The first interface has 24 pins that can be used as ADC digital inputs: ADC_A[0:11] and ADC_B[0:11] or as DAC digital output DAC_I[0:11] and DAC_Q[0:11]. In both cases, the data is clocked by the ADC CLKIN single ended clock input.

The AFE is a mixed signal core that has all the blocks of mixed-signal design required for the PVG610. It integrates the following blocks:

- Dual baseband 12-bit ADC 200MHz
- IF sampling 10-bit ADC 200MHz
- Dual baseband 12-bit DAC 200MHz
- Envelope 10-bit ADC 60MHz

3.6.4 Rx Demodulator

The Rx Demodulator is comprised of the following sub-blocks:

- Digital Tuner
- Symbol Synchronization
- Frame Synchronization
- Equalization
- Carrier Synchronization

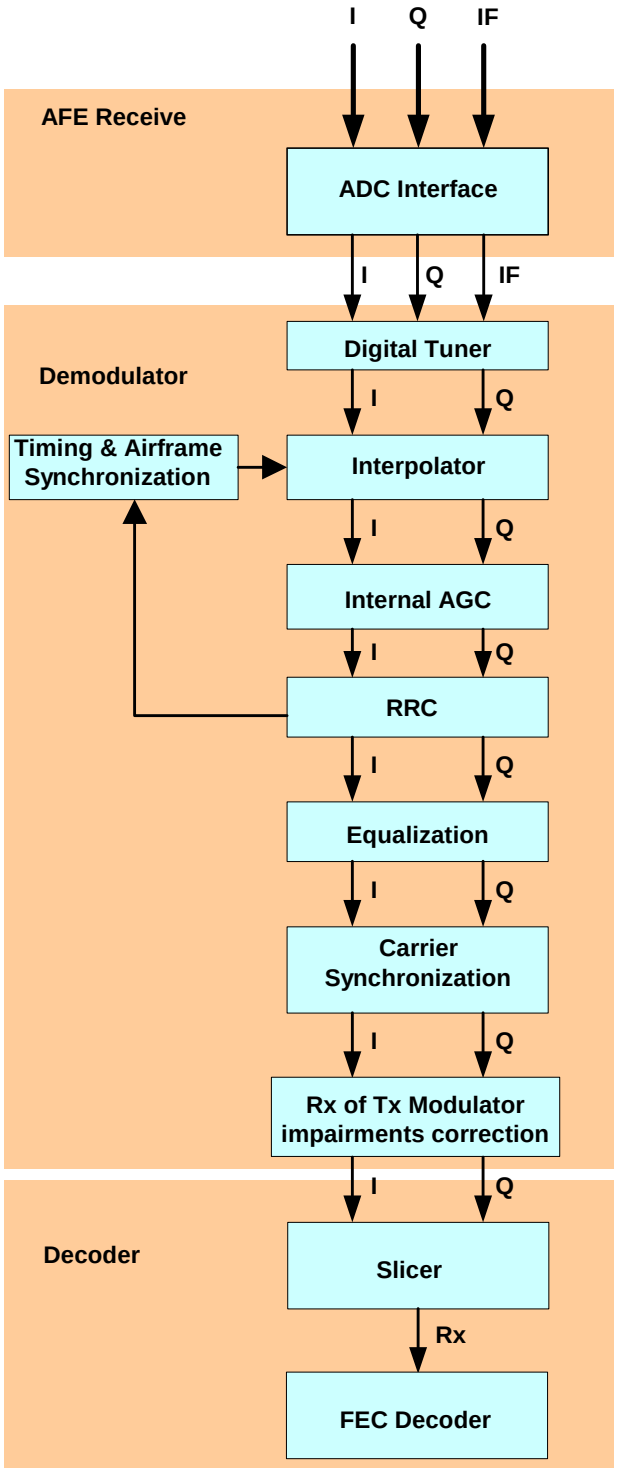


Figure 33: Demodulator Block Diagram

3.6.4.1 Digital Tuner

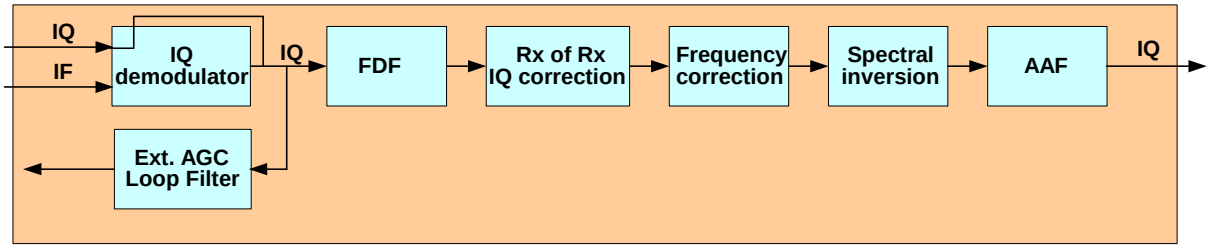


Figure 34: Digital Tuner Block

3.6.4.1.1 IQ Demodulator

The IQ demodulator converts a sampled IF carrier to I and Q components. The IF carrier can be centered at a frequency of Fsample/4 or at any odd multiple of that frequency (3/4 Fsample, 5/4 Fsample, etc.). If IQ lines are received the IQ demodulator is bypassed.

3.6.4.1.2 External AGC Loop

The AGC Loop is connected to external Variable Gain Amplifier (via PWM signal). It preserves constant RMS in the ADC input with a second order loop. The AGC has two sets of loop parameters: one for acquisition and the other for tracking. Both sets are configurable.

3.6.4.1.3 FDF

The FDF is a real filter with 14 taps FIR filter, placed on the Q rail, thus enabling a delay of a fraction of an integer. The I rail is delayed by an integer number.

The FDF has two functions:

When using IF synthesis, it ensures offset of half a sample between I and Q samples.

When using baseband modulation, it compensates on any delay between I and Q rails up to ±7 samples

3.6.4.1.4 I/Q Impairments Correction (Rx of Rx)

The Rx of RX IQ Imbalance Correction corrects gain, phase and DC leakage IQ imbalances, caused by the receiver IQ demodulation. The algorithm used in this module is blind. The quadrature and DC correction performed with this module is done by an adaptive algorithm, which estimates I and Q Imbalances. The algorithm is implemented both in SW and HW in a way that the SW generates a set of correction coefficients based on HW estimators.

3.6.4.1.5 Frequency Correction

The frequency correction module is used to shift the receiver carrier frequency by a moderate amount. The frequency driving the Number Control Oscillator (NCO) is programmable within a range of ±Fsample, which allows a modulated carrier to be shifted by:

For baseband sampling: ± [0.8*Fsample/2 - (1+α)*Fbaud/2]

For IF sampling: ± [0.8*Fsample/4 - (1+α)*Fbaud/2]

Since mixing the input signal may result an overflow, an output scalar may be used to prevent saturation.

A sweep mechanism enables slow shift from the current frequency to the desired one.

3.6.4.1.6 Spectral Inversion

Applying complex conjugation to the Q rail results in spectral inversion. When using the internal digital Inphase Quadrature (IQ) modulator, spectral inversion is sometimes required (e.g., when the image around 5/4 Fsample is selected). Depending on the design of the transmitter RF chain, spectral inversion may also be useful for external analog IQ modulation.

3.6.4.1.7 AAF

The Anti-Aliasing Filter (AAF) bank is a decimation and filtering stage designed to support decimation ratios of up to 16:1. An additional decimation factor of up to 3 is available from the interpolation stage of the receiver.

The AAF module consists of four decimate-by-2 stages and an additional antialiasing filter designed to prevent aliasing at the next interpolation stage.

Each decimation module is built from a 17-tap symmetric programmable FIR filter that outputs only decimated samples (i.e., output rate is half the input rate). Coefficients are <10,9> signed fractions except for the center tap,

which is fixed at 1.0. The last filtering stage (AAF5) does not include the decimation facility but it is otherwise identical.

At each AAF output there is an AGC component to enable full scale while entering the next AAF.

3.6.4.2 Rx Interpolator

The Rx interpolator reduces the data rate from the AAF sampling rate to twice the symbol rate. The interpolation filter is controlled by the timing loop. In XPIC configuration, the slave interpolation filter is controlled by the master's timing loop.

3.6.4.3 Internal AGC

The internal AGC adjusts the signal's RMS level to achieve optimal SNR. The AGC loop is a second order loop. Nevertheless, typically the loop is configured to work as first order. The AGC has two sets of loop parameters: one for acquisition and the other for tracking. Both sets are configurable.

3.6.4.4 RRC

This is a squared Root Raised Cosine filter.

3.6.4.5 Symbol Timing Synchronization

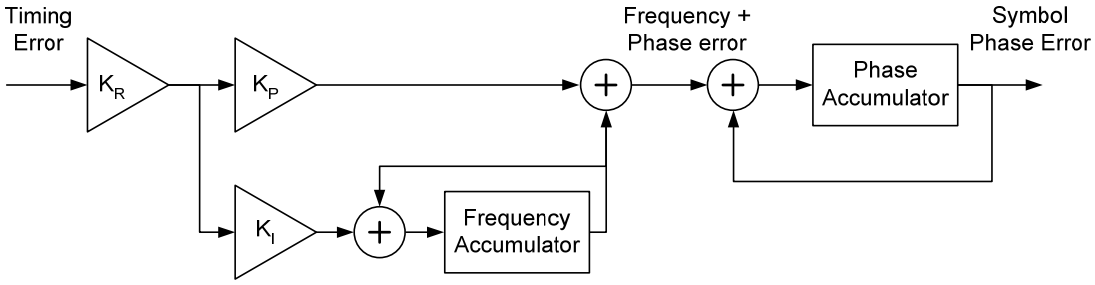


Figure 35: Symbol Synchronization Block Diagram

Symbol timing synchronization is detected after the Rx RRC filter. The timing error is calculated as follows:

TE = (IN+2 - IN) IN+1 + (QN+2 - QN) QN+1

The Symbol timing synchronization system uses a second order loop to track the symbol timing. The phase of the symbol timing drives the Rx Interpolation filter so that it generates two complex samples per symbol. One sample represents the peak of the eye-opening symbol and the other the transition point.

The symbol synchronization block also includes internal AGC mechanism which preserves constant RMS with a second order loop. The AGC has two sets of loop parameters: one for acquisition and the other for tracking. Both sets are configurable.

3.6.4.6 Frame Synchronization

This block identifies the airframe start. The block functions in the following modes:

3.6.4.6.1 Preamble Modes

A preamble correlator filter locks on the preamble. Once the first preamble is detected the state machine can be programmed to search for additional preambles, or declare modem locked.

When ACM is in use, the airframe size is not fixed and the correlator extracts the airframe size from the ACM header. When ACM is not in use the airframe size is fixed.

The correlator keeps searching for the preamble on each airframe even when the modem is locked. When a configurable number of times the preamble is not found the correlator declares loss of lock.

Remark –TDD mode always requires a preamble

3.6.4.6.2 Backward Compatible Modes

The preamble is not a part of the airframe.

A byte correlator is locked on specific pre-defined sync bytes.

The sync bytes appear as a header in the beginning of each RS block.

3.6.4.7 Equalization

Two equalizer sections are provided for the removal of inter-symbol interference, a 24-tap T/2 spaced feed-forward filter (FFF) and a 3-tap decision feedback filter (DFE). During acquisition, the feed forward section may use CMA adaptation and switch to the decision-directed adaptation after carrier lock and sufficient convergence. Another option is to use decision–directed adaptation over the pilots and the preamble.

The DFE adaptation is decision-directed and may be activated after the FFF has converged. The DFE can be activated for the PVG310 backward compatible mode or for the PVG610A airframe mode when pilots are not used.

The weight update coefficient, μ, and the leakage coefficient, β, are programmable for each filter.

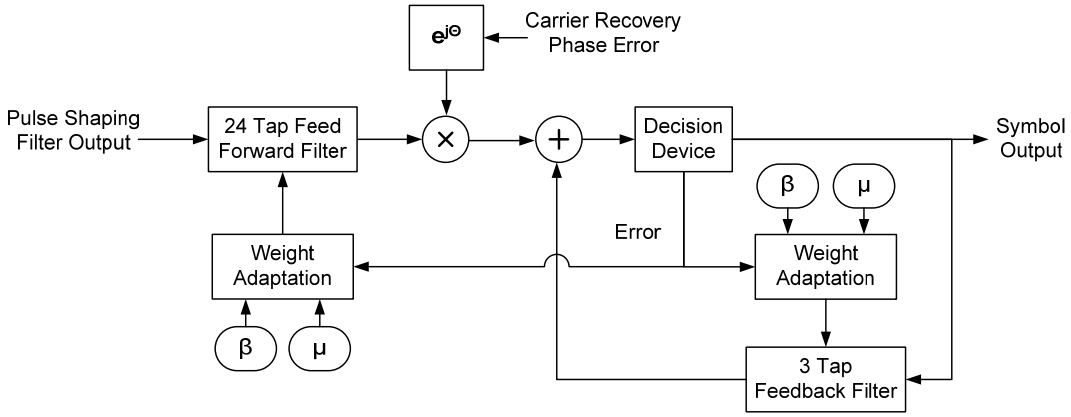


Figure 36: Equalizer Structure

The FFF is a T/2 spaced complex asymmetric filter (where T is a symbol interval). The filter performs decimation by 2; two samples are shifted in for each symbol produced at the output.

The FFF supports 24 complex coefficients with 16 bits of precision.

Two adaptation algorithms are supported:

Blind adaptation based on the Constant Modulus Algorithm (CMA)

Decision directed LMS, where the filter coefficients are adapted to minimize the Mean Squared Error (MSE) at the slicer input. The tap leakage algorithm is used to improve numerical stability.

The Decision Feedback Equalizer (DFE) is an adaptive T-spaced complex filter. The filter has three complex coefficients with 16-bit precision.

The coefficients of the filter may be adapted only when the equalizer is operating in a Least Mean Squares (LMS) mode.

The tap leakage algorithm is used to improve numerical stability.

3.6.4.8 Carrier Synchronization

The carrier Synchronization loop tracks the phase error at the Feed Forward Filter (FFF) output. The circuit is a 2nd order digital phase locked loop operating at the symbol rate. The phase detector of this PLL is decision directed (i.e., based on decisions made in the slicer).

The digital implementation has only a 4-symbol delay and uses the same slicer to adapt the equalizer coefficients.

The carrier loop supports a range of loop bandwidths designed to maximize phase noise tracking capability and minimize the effect of thermal noise. Optimization of the loop depends on expected SNR, phase noise, etc.

The Carrier Synchronization block also includes a Pilot Symbol Assisted Modulation (PSAM) mechanism, estimating the phase noise based on pre-defined seeded pilots in the symbol chain. A priori lookup table of RAM pilots is used to modulate the pilot symbols at the transmitter side. The phase is smoothened at the receiver side and used to estimate phase correction.

3.6.4.9 Correction of modulator impairments (Rx of Tx)

This block corrects modulator impairments that were not corrected by the Tx of Tx mechanism (either because Tx of Tx is not used or because residual impairments are uncorrected by the Tx of Tx).

Note: The Rx of Tx block can not be used when digital Tx frequency correction is used.

3.6.5 Rx Decoder Description

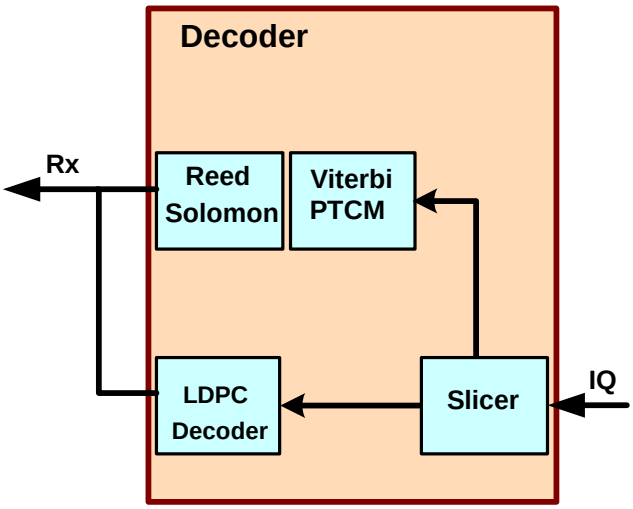


Figure 37: Decoder Block Diagram

3.6.5.1 Slicer

3.6.5.1.1 Soft Slicer

The soft slicer determines the Log Likelihood Ratios (LLR) for incoming bits. There are two types of LLRs; one is used as soft inputs for the LDPC decoder and the other for the Viterbi decoder.

3.6.5.1.2 Hard Slicer

The hard slicer is a simple programmable 16x16 lookup table. It translates symbols to bits that may be used for uncoded system tests or with the RS decoder. It can support all constellations from QPSK to 256QAM as long as the constellation points are spaced on a simple rectangular grid. Non-rectangular constellations such as 128QAM are treated in a sub-optimal manner. However, the degradation in performance is negligible. For correct operation, both the lookup table and the normalizer parameters is used.

3.6.5.2 Viterbi PTCM Decoders

3.6.5.2.1 Viterbi Decoder

The inner decoder module implements Viterbi decoding, Trellis decoding, and hard decoding. The decoder is programmable and supports several coding schemes. Some functions are also available for synchronizing the decoder under software control. The following table lists the codes supported by the Inner Code Decoder (ICD) module.

Table 8: List of Codes supported by the ICD Modules

Modulation	Code Type	Rate
QPSK, 16-32-64-128-256 QAM	No code. Hard slicing	N/A
QPSK	Conventional	1/2, 2/3, 3/4, 5/6, 7/8
16QAM	2D-Trellis	3/4
16QAM	4D-Trellis	7/8
32QAM	4D-Trellis	9/10
64QAM	2D-Trellis	5/6
64QAM	4D-Trellis	11/12
128QAM	2D-Trellis	6/7
128QAM	4D-Trellis	13/14
256QAM	2D-Trellis	7/8

The Viterbi decoder is the industry standard 64-state rate 1/2 convolution decoder. Viterbi decoding is based on Log Likelihood Ratios of the received bits. Two LLRs are produced per QPSK symbol by the depuncturer unit.

The decoder trace back memory to at least 128 bits. A depuncturer is used to support higher rate codes.

Viterbi decoder: accepts LLRs and produces decoded bits.

PTCM decoder, A Trellis decoder: accepts symbols and produces decoded bits.

The depuncturer prepares LLRs for actual decoding by filling in punctured bits. It can search for a correct depuncturer phase under software control.

3.6.5.2.2 PTCM Decoder

The Trellis decoder is based on the Punctured Pragmatic Trellis approach introduced by Wolf and Zehavi (IEEE Comm. Magazine, Feb. 1995).

The decoder uses the 64-state rate 1/2 Viterbi decoder to decode 2D and 4D Trellis codes. Several programmable lookup tables assist in computing Euclidean distances.

3.6.5.3 Sync Byte Description

For modes without preamble, the final synchronizer (see Frame synchronization 3.6.4.6) that goes through the decoded byte stream looks for sync bytes. The decoder outputs a synchronized byte stream with the synchronization bytes flagged for further synchronization of subsequent modules.

The sync byte detector state machine looks for sync bytes and inverted sync bytes in the decoded bit stream.

When a configurable number of sync bytes at expected intervals (one code word apart) are detected, the decoder is considered to be synchronized and starts producing data bytes.

Similarly, when the state machine misses a configurable number of sync bytes, it declares a loss of synchronization, stops producing output bytes, and resumes searching.

3.6.5.4 De-Interleaver Description

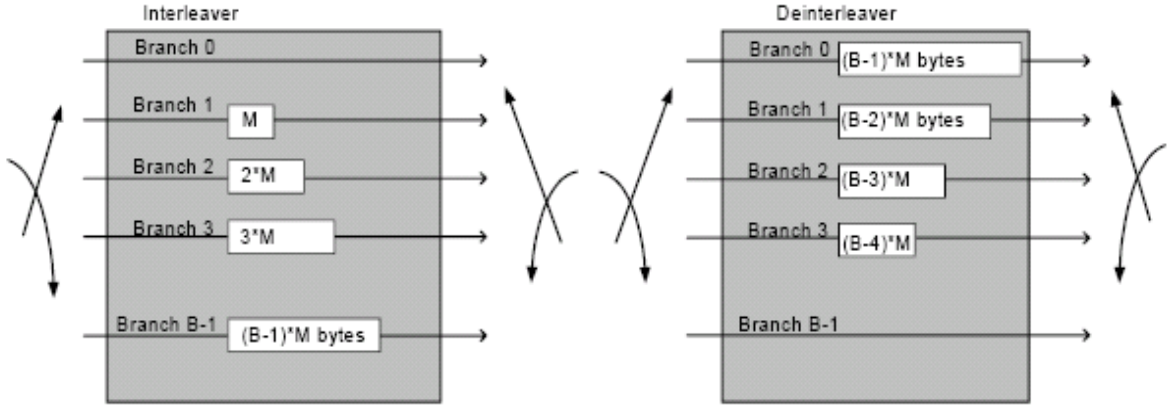


Figure 38: De-interleaver Block Diagram

The de-interleaver module implements a convolutional de-interleaver with programmable depth and span. De-interleaving is performed after (optional) Trellis decoding and before RS decoding. The interleaving/deinterleaving process is designed to spread bursts of errors over multiple code words, thus increasing the likelihood that the RS decoder will be able to correct the errors.

Interleaver of depth B and span N can spread a burst of B erroneous bytes over B different code words of size N bytes. The interleaving/de-interleaving process adds a total delay of N*(B-1) bytes to the link.

The deinterleaver is automatically synchronized by routing sync bytes from the sync-byte-detector to branch 0.

3.6.5.5 Reed Solomon Block Description

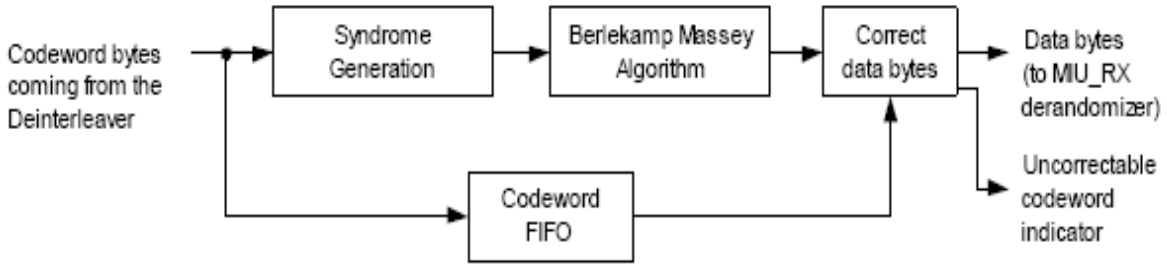


Figure 39: Reed Solomon Block Diagram

The Reed Solomon (RS) decoder receives de-interleaved codewords, attempts to correct byte errors, and strips off the redundant bytes. The RS code is a shortened, systematic code over GF(256). Codeword length (N) is programmable up to 255 bytes.

Redundancy (R) is programmable up to 32 bytes. The decoder can correct up to T erroneous bytes, where T is half the number of redundant bytes (T=R/2).

Code Generator Polynomial: g(x) = (x+μ0)(x+μ1)(x+μ2)... (x+μ2T-1), where μ= 0x02

Field Generator Polynomial: $p(x) = x^8 + x^4 + x^3 + x^2 + 1$

The decoder is based on the Berlekamp-Massey algorithm and can correct at most, T errors. When more than T errors occur, the decoder may not detect the error locations correctly and thus may incur additional T errors (worst case scenario). Sometimes, the decoder is able to determine that a codeword is not correctable after it has been processed. In this case, the decoder flags all bytes of the codeword as 'uncorrectable'. This output is available as a dedicated output pin of the modem.

To permit estimation of channel quality during normal operation, the decoder maintains two counters: one is counting the number of errors detected so far, and the other is counting the total number of bytes processed.

The decoder synchronization is based on the embedded sync bytes and is handled automatically.

3.6.5.6 LDPC Decoder

The decoder is based on Z parallel processors that decode Z-bits simultaneously. The parallel processor factor is 84. The LDPC code supports various code rates (with ~0.1%-1% granularity). These rates are obtained by puncturing the codeword (in the encoder) by np bits. The punctured code is based on puncturing either a mother code of rate ¾ or a mother code orate of ½. Thus, it is possible to achieve code rates between 0.5 to approximately 0.95.

The supported codeword lengths are:

n = 2016, 4032, 8064 and 16128.

All parameters are summarized in the following table.

Table 9: LDPC Code Rates

n	R(Rate)
2016	0.5
	0.75
4032	0.50
	0.75
8064	0.50
	0.75
16128	0.50
	0.75

3.6.5.6.1 Decoding Algorithm

The decoding algorithm is an iterative message passing decoding scheme. This algorithm relies on the graph-based representation of the code. Messages are passed from the left side to the right and response messages are passed from the right side to the left side. Every iteration of the message-passing algorithm, each variable code in the graph passes a message to its connected check node. Each check node accumulates all messages received and then replies to each variable node.

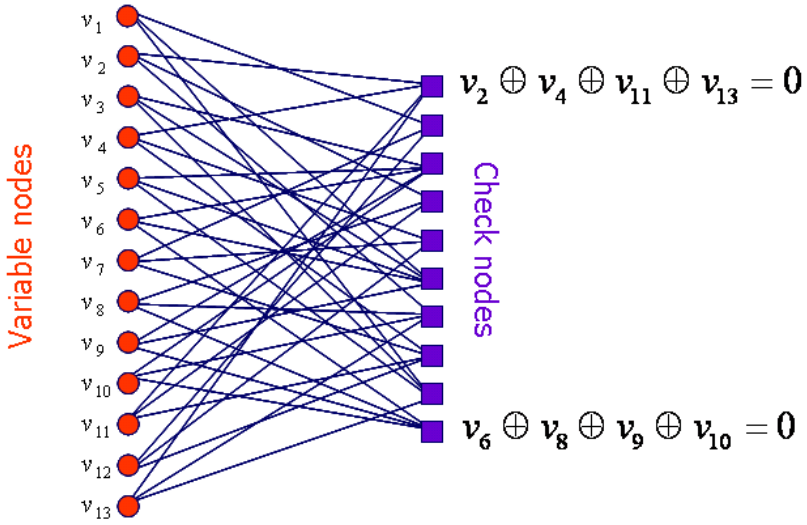


Figure 40: Variable Nodes

The iterations are repeated until either convergence is attained, or the number of iterations reached a pre-defined maximum, whichever occurs first. If the number of iterations reached the pre-defined maximum and there was no convergence a dedicated uncorrectable pin is raised

The serial decoding schedule is as follows:

Initialization:

All the variable nodes are initialized with a log likelihood ratio based on the received symbols. Hence the initial metrics assigned to all variable nodes at the tanner graph, assume a prior knowledge of the noise level in the channel.

Iterations:

Each variable node sends a message QV - RCV to a check node. QV is the current metric held in the variable node v and represents the reliability of each received bit, i.e. the larger the Qv is (towards plus infinity) the more likely that this bit is 0 and not 1 and vice versa. RCV is the previous message (in the previous iteration in the opposite direction).

Each check node sums all the messages sent from all the variable nodes connected to it (after converting these messages from the probability domain to the log domain). This sum represents the reliability of a row check in H The update (response) that a check node C sends back to a variable node V is a conversion of the sum excluding the message from the current node (converted from log domain to probability domain). This is the intrinsic property of the algorithm, i.e. an outgoing message from a node (either from the left side or from the right side) is a function of the other incoming messages not including the message on the outgoing arc.

This update is added to the previous reliability of the variable node QV ← QTEMP + RCV The algorithm goes over all the check nodes and updates the variable nodes which are connected to this check node. This is done serially until all the check nodes are processed (all rows of H have been checked). This concludes one iteration.

The algorithm continues until either convergence is attained or the number of iterations has reached a pre-defined maximum value, which ever occurs first. Whenever the max iteration

3.6.5.6.2 Non Multi-level Decoding

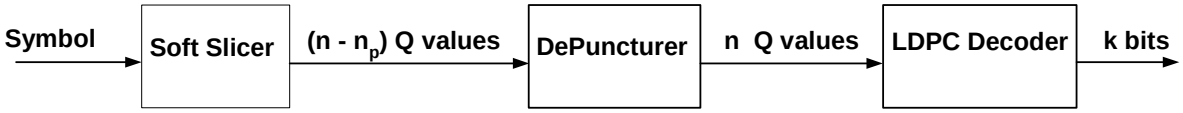


Figure 41: LDPC Non-Multi-Level Decoding

Upon receiving a symbol, the soft slicer calculates log2 N LLRs. The number of symbols, that constitute one LDPC codeword, is (n-np)/log2N. Thus, the number of LLRs, which are calculated, is (n-np) Next, these LLRs are depunctured in np indices (a zero is placed in the puncturing indices), yielding n LLRs. These n LLRs are written into the Q-memory of the LDPC decoder, which in turn produces a decoded information word of k bits.

3.6.5.6.3 Multi-level Decoding

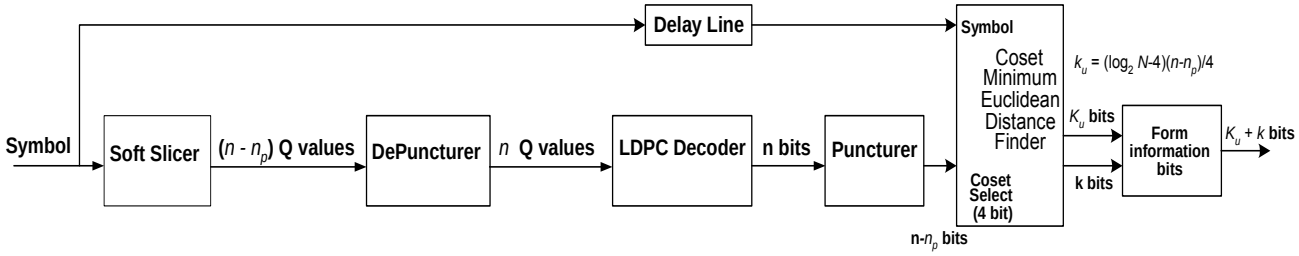


Figure 42: LDPC Multi-level Decoding

Upon receiving a symbol, the soft slicer calculates 4 LLRs for the 4 coded bits. The number of symbols, which constitute one LDPC codeword, is (n-np)/4 Thus, the number of LLRs, which are calculated, is (n-np) Next, these LLRs are de-punctured in np indices (a zero is placed in the puncturing indices), yielding n LLRs. These n LLRs are written into the Q-memory of the LDPC decoder, which in turn produces a decoded codeword of n bits. Unlike Non-Multi-Level mode, in which, the LDPC decoder discards the parity bits and provides only k information bits, in Multi-Level mode, the LDPC decoder provides n bits, i.e. both information bits and parity bits are needed. The first k bits out of these n bits are information bits, which are part of the final output (decoded word).

The uncoded bits are extracted from the symbols by taking minimum Euclidean distance decisions. The n bits are punctured at and the remaining (n-np) bits out of n LDPC decoded bits are divided into groups of 4 bits. Each group selects a coset in the constellation, in which minimum Euclidean distance decisions are taken. These decisions are near optimum decoding of the uncoded bits. The group size of un-coded bits is (log2 (ConstallationOrder)-4) bits. There are (n-np)/4 such groups (as the number of symbols), thus the number of decoded un-coded bits is ku=(log2N-4)(n-np)/4 The output of the decoding is k+ku bits, which are the exact number of transmitted information bits.

3.7 Controller Block Description

3.7.1 CPU Block Diagram

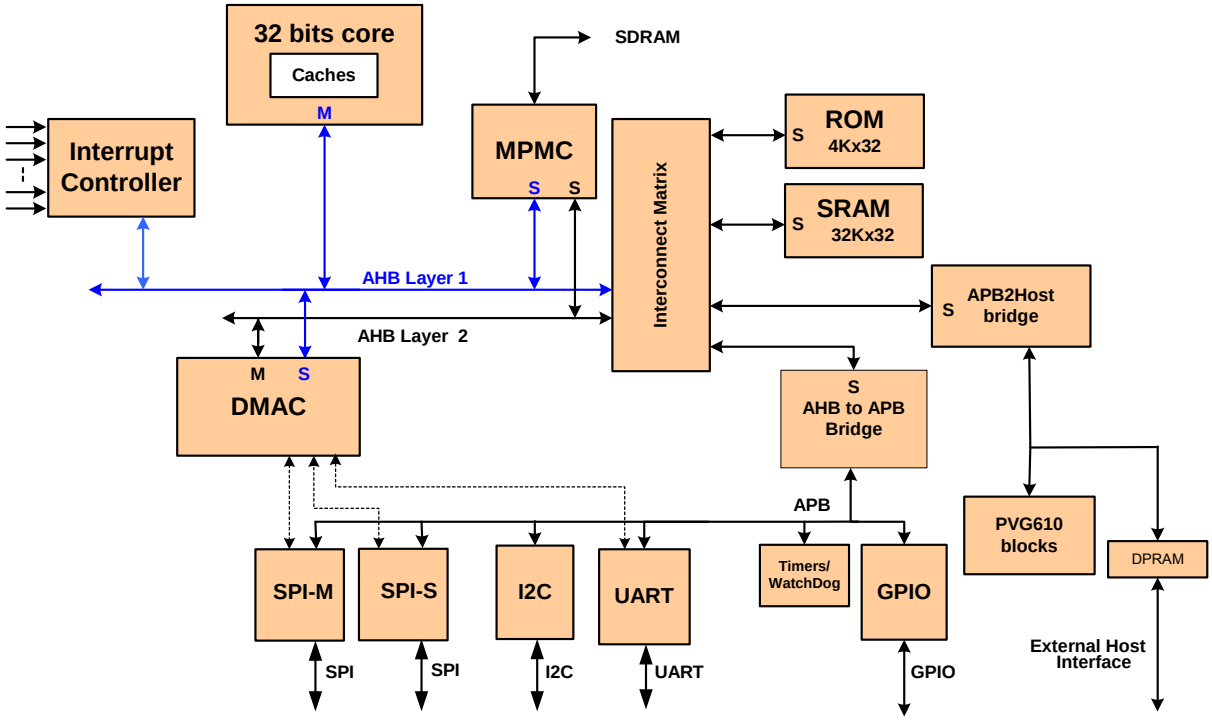


Figure 43: CPU Core Architecture

3.7.1.1 CPU core

PVG610A CPU is an ARM926E-S model, with instruction and data caches, Memory Management Unit (MMU) and AMBA (Advanced Microprocessor Bus Architecture) AHB (Advanced High performance Bus) interface.

It is a high performance 32-bit System on Chip (SoC) processor.

- Memory and Buses:
- Instruction cache size – 8Kbyte
- Data cache size – 8Kbyte
- SRAM size – 128Kbyte.
- ROM size – 16Kbyte
- Core speed of up to 200MHz.
- AHB bus speed of up to100MHz.
- APB bus speed of up to100MHz
- Option for external SDRAM

3.7.1.2 CPU peripherals

The following peripherals are included in the SoC processor:

- UART interface
- I2C interface
- SPI interfaces (master and slave)
- GPI/O interfaces
- Host interface to external CPU
- Timers
- Watchdog
- Interrupt controller

3.7.2 Host Interrupt

The HOST_INT output signal is used as a central interrupt for the PVG610, toward an external CPU. This signal combines interrupts from multiple sources within the PVG610, including software events, networking events and physical layer indicators.

The host interrupt signal is software controlled.

The host interrupt signal is active low.

3.7.3 Watch dog

The PVG610A has three watchdog (WD) operating modes. In all of them the time out and patting time are configurable:

3.7.3.1 Internal mode

The internal watch-dog block in the PVG610A resets the internal CPU as the WD indication is set. No external devices or logic are needed

3.7.3.2 External Mode 1

The WD signal is set (Low to high) indicating CPU reset is required. In this mode an external device resets the CPU using CPU_NRESET signal.

3.7.3.3 External Mode 2

The WD signal functions as WD clock that stops patting as the SW fails. The patting signal is an active high pulse with a width of 64 System Clock cycles. This signal can be used to implement external WD timer or to use WD timer device that produces the reset signal.

4 Adaptive Code and Modulation (ACM)

4.1 ACM General Functionality

The PVG610A supports ACM in which coding rate and modulation changes are set in real time, based on the link conditions. This feature enables to significantly increase the payload capacity and link availability. When the link's SNR is high, e.g. during good weather condition, the link capacity is high enabling full operation of all applications. In case that the link's SNR drops significantly, e.g. during heavy rain, the link capacity is reduced. The PVG610A ACM uses the class of service methodology to define which services is fully provided regardless of the link condition, and which services level is modified or stopped whenever the link condition is degraded.

The figure below shows the channel capacity changes due to SNR level and the services capacity adaptation.

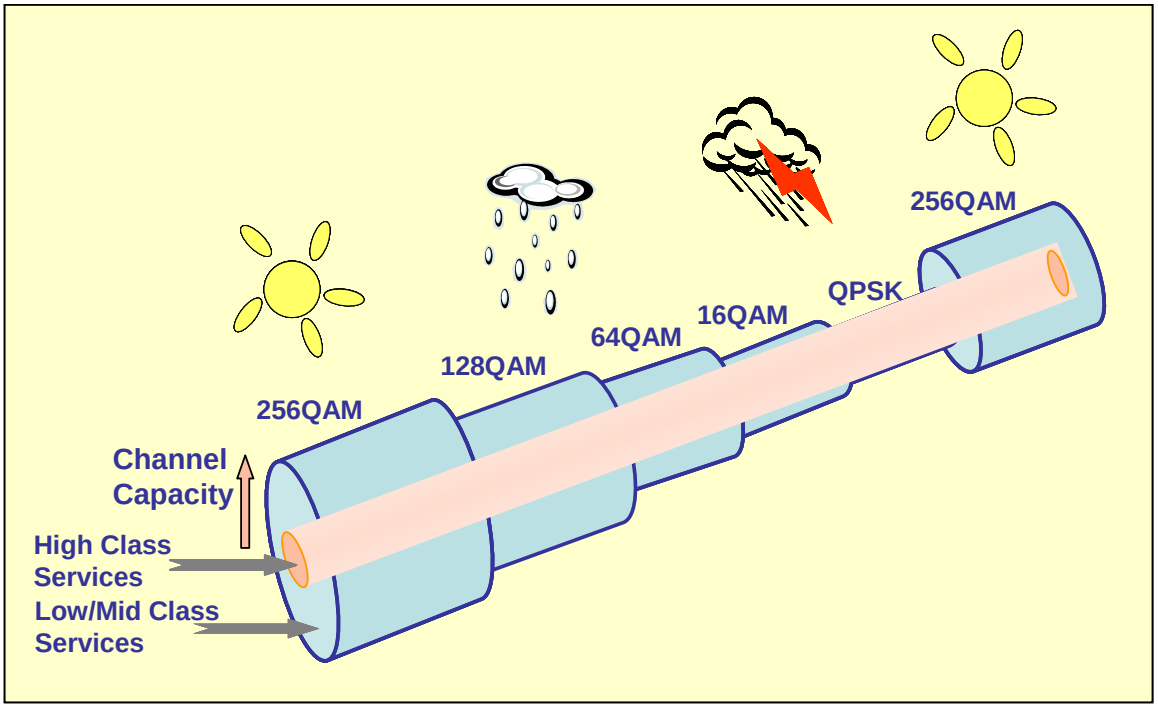


Figure 44: Channel Capacity Variation

Switching from one modulation and coding rate to another is conducted hitless, and is fully managed by the PVG610.

An ACM profile defines both the physical layer parameters (such as modulation and FEC) and the networking layer parameters (such as the number of E1s used in every ACM profile) for a given channel conditions (such as signal-to-noise ratio (SNR) range. The channel conditions range set for each profile is used for determining when to perform a switch from one ACM profile to another. Each ACM profile has a different spectral efficiency, derived from its modulation and FEC, as shown in the figure above. For example, the ACM profile with 128QAM modulation (and appropriate coding) in the diagram can be configured for an SNR range of 21-24dB, enabling spectral efficiency of approximately (pending on the coding rate) 6 bits-per-Hz. When the channel conditions degrade, i.e., when the SNR is below 21dB, a different and suitable ACM profile is used. For example, for an SNR range of 9-12dB an ACM profile with 16QAM modulation (and appropriate coding) may be used with spectral efficiency of approximately 3bits-per-Hz (pending on the coding rate).

An ACM profile is linked to the data rate of each service. It assures that high-class services are allocated with the required bandwidth with high availability. It also assures appropriate bandwidth allocation, based on the link condition, to other services levels.

The ACM implementation supports various modes of operations:

Data Multiplexing with a General Purpose Multiplexer (GPM) – the PVG610A integrated GPM is used and switching to a new ACM profile, which consists both physical layer and data layer parameters, is done completely inside the PVG610.

GPI mode – the PVG610A is in charge of switching the physical layer from one ACM profile to another. The PVG610A also switches from the rate over the GPI. In this mode, the switching of the ACM profile in the data layer, e.g., which tributaries are drop or added is done externally.

ACM engine – The ACM engine is the logic which makes the decision on when to switch an ACM profile. This logic may be implemented using the internal PVG610A firmware and is referred to as internal ACM engine. It can also be implemented outside the PVG610A either by an external FPGA or by SW running in the host

When the embedded (internal) ACM engine is in use, the Switching command from the receiver side is conveyed to the transmitter side via the IMB channel. As the transmitter receives the ACM profile it switches to it immediately. The receiver is notified that the switch was executed using dedicated bytes on the GPM (if used) and airframe headers.

The receiver can output notification notice (externally) on ACM switching via the GPI interface. The transmitter can output pre-notification (externally) on the ACM profile switching (via the GPI interface), up to 8 airframes (configurable) before the actual switching. This notification/pre-notification enables the user to arrange its received/transmitted data according to the new ACM profile limitations.

When an external multiplexer is in use, and/or external ACM engine is used, the ACM switching command from the receiver end to the transmitter end is conveyed by the external framer. For this case, when the ACM engine is internal the external framer must provide a channel to allow communication of the PVG610s between the two ends of the link. To pass messages from one end of the link to the other the PVG610A is connected to the external framer with serial HDLC which passes the message to the de-framer on the other end of the link which in turn passes the message to the PVG610A on the other end of the link through an additional HDLC channel

PVG610's internal embedded ACM engine can be configured with up to 16 different ACM profiles. The ACM profiles are defined in the configuration file, and loaded to the PVG610A after HW reset. Except for the profile in use, the ACM profiles can also be modified during run time by the host using the API commands.

Whenever an external ACM engine is in use, the PVG610A provides direct HW access to various indicators, enabling the external ACM engine to monitor the indicators and thus to be able to make decisions on whether to switch to a new ACM profile. The external ACM engine can control the ACM switching via APIs. The ACM APIs also enable the host to define ACM profiles, define a range or a specific ACM profile to be in use, and to get ACM status from the PVG610.

4.2 Estimating ACM Factor

The receiver side is constantly monitoring the link condition on various estimators. Thresholds may be set on these estimators to cause an interrupt when the thresholds are crossed. The decision algorithm for switching an ACM profile varies from one algorithm to another. For example, it can be based on crossing either an indicator threshold.

Some algorithms use a combination of more than one indicator to improve the ACM switching performance and reliability. The ACM decision algorithm usually includes hysteresis to avoid undesired back and forth switching in cases where the estimators' level jitters between two ACM profiles.

The ACM switching rate, measured in dB-per-second, is a dominant factor in ACM systems; the higher the switching rate, the better the system's immunity to rapid SNR changes. When the switching is being executed, the payload rate is being modified to fit the aggregated data rate to the new available link data rate.

The following are means of estimating the SNR for selecting the ACM.

4.2.1 Radial MSE indicator

The Radial MSE indicator is a phase noise invariant method for estimating the signal to noise ratio.

The estimator $\hat{\sigma}_r^2$ is based on averaging the squared radius difference of the received signal and the hard decision signal $\hat{\sigma}_r^2 = E\left(|y| - |\hat{s}|\right)^2$.

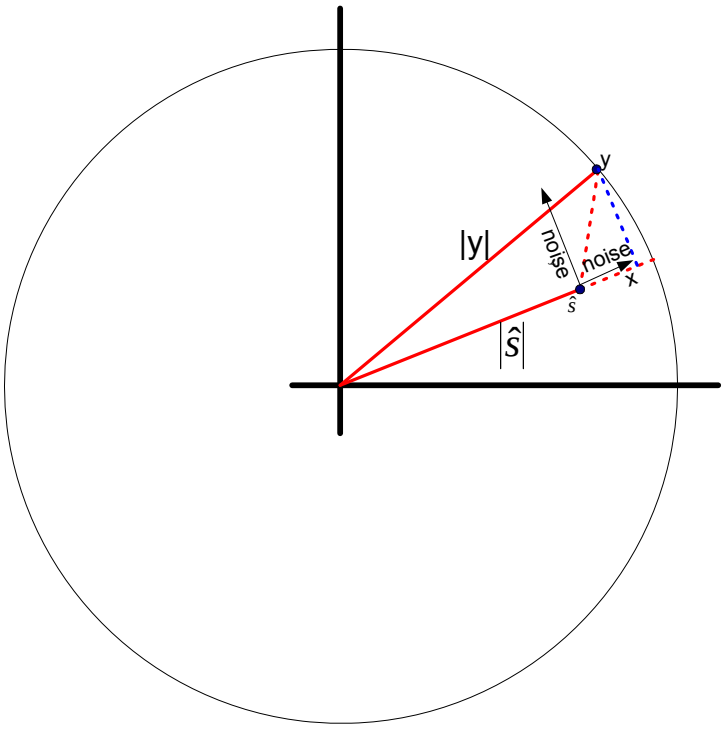


Figure 45: Radial MSE indicator

4.2.2 Total MSE estimator

This estimator compares the in-out of the slicer and averages the square of them. It estimates the sum of thermal noise variance and the residual phase noise variance.

$$\hat{\sigma}_r^2 = E\left(\left|y - \hat{s}\right|^2\right)$$

4.2.3 LDPC Decoder Stress

The LDPC is monitored for the number of errors being corrected. The number helps estimation the ACM level to be selected.

4.3 Symmetric and Asymmetric Modes

In symmetric operation, ACM switching is coordinated so that both directions of the link switch together, keeping a symmetric capacity on both channel directions. Whenever it is required to reduce the spectral efficiency in one channel direction the other channel direction is reduced as well.

In Asymmetric Mode, each channel direction has its own independent ACM engine, allowing different capacity on each channel direction. It is thus possible that one channel reduces its spectral efficiency, while the other channel direction enjoys high spectral efficiency.

5 Airframes and Modes

5.1 Airframe Types

There are two airframe types in PVG610;

- PVG610A airframe, supporting PVG610A features
- PVG310 compatible airframe, supporting interoperability with PVG310 based system

5.1.1 PVG610A Airframe

The airframe is a frame of sequential symbols transmitted from a source PVG610A to a destination PVG610. A fully configured airframe has a preamble field followed by an ACM field, then followed with payload field with inserted pilots in equal symbol spacing. The basic airframe configuration contains a preamble and a payload field. ACM and pilot fields are optionally configured.

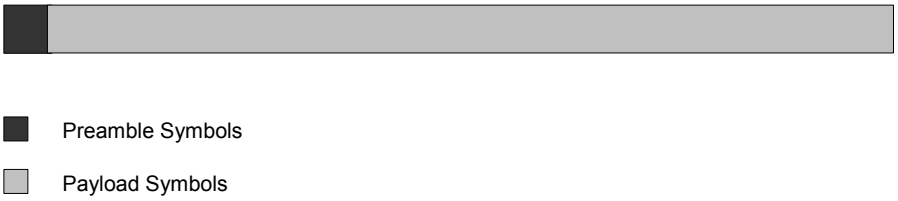


Figure 46: Basic Airframe Configuration

Figure 47: Full Airframe Configuration

Each of the fields is further described below.

5.1.1.1 Preamble Symbols

The preamble is a sequence of QPSK symbols (32 or 16) used for modem synchronization and adaptation of carrier loop recovery, symbol timing loop and other adaptive loops.

5.1.1.2 ACM Symbols

The ACM field consists of 16 symbols which define the ACM profile. There are 16 possible ACM profiles. Each profile is defined by modulation, coding rate, active tributaries and other parameters. For detailed description of ACM see Chapter 4.

The ACM field is optional.

5.1.1.3 Payload Symbols

The payload contains data and FEC. An airframe contains 1 to 16 code blocks (LDPC or RS).

5.1.1.4 Pilot Symbols

Pilots are inserted in equal and configurable symbols spacing in the payload. The pilots are QPSK symbols taken from a cyclic fixed series. Pilots are mainly used for enhanced phase noise immunity and are also used for improved adaptation of various adaptive loops.

The use of pilots is optional.

5.1.2 PVG310 Compatible Airframe

The PVG310 frame consists of a sync byte followed by a data block. The PVG310 super frame consists of eight frames. The sync byte of the last frame is inverted, see drawing below.

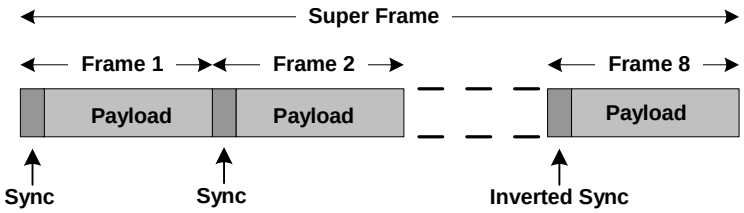


Figure 48: PVG310 Compatible Frame

5.1.2.1 Sync

The sync is a single constant byte used for modem synchronization. The inverted sync used for super frame synchronization is a binary inversion of the sync byte.

5.1.2.2 Payload Symbols

The payload contains data and FEC.

5.2 Operation Mode Types

The PVG610A transceiver operates in three modes;

- FDD - Frequency Division Duplex, transmit and receive concurrently in different frequencies
- TDD – Time Division Duplex, transmit and receive in the same frequency but in different time slots
- XPIC - Cross Polarization Interference Cancellation, transmit and receive in different frequencies whereas the transmitter and receiver use two orthogonal polarizations.

5.2.1 Frequency Division Duplex (FDD)

A PVG610A operates as a transmitter and as a receiver. In FDD mode the transmitted frequency is different than the received frequency. Hence, the transmitter and receiver operate simultaneously.

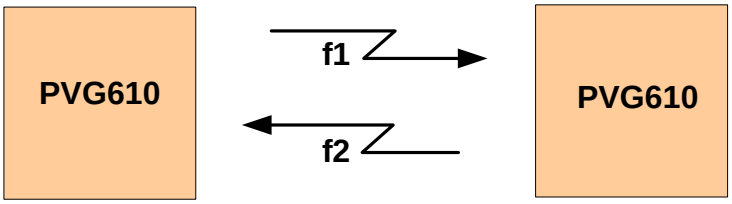


Figure 49: FDD mode

5.2.2 Time Division Duplex (TDD)

Transmit and receive in TDD share the same frequency whereas division is made over time. A TDD frame consists of two airframes – Tx frame and Rx frame. The size of the Tx and Rx frames is not necessarily identical. A TDD frame may have Tx/Rx time division of 50/50, 80/20 or others.

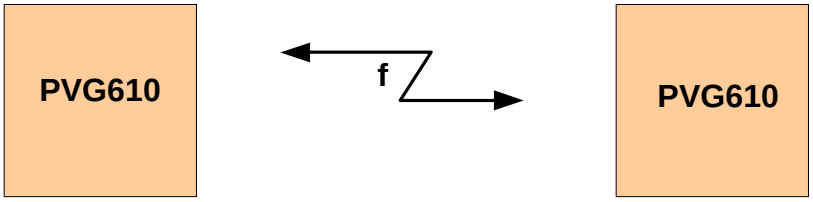


Figure 50: TDD

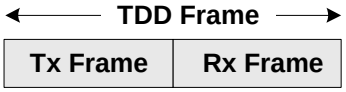


Figure 51: TDD Frame

5.2.3 XPIC Mode

The XPIC mode is implemented with PVG610X models.

Channel capacity can be doubled with very little performance degradation, operating in XPIC mode in which horizontal and vertical antenna polarizations are used. The XPIC mode is a variation of the FDD mode. Two PVG610X units independently transmit different payloads at orthogonal polarization (with respect to each other) at the same frequency band. Similarly two PVG610X, referred as master, units independently receive different payloads at orthogonal polarization at the same frequency band. In order to cancel interference between the orthogonal polarizations there is a need for two additional PVG610X (altogether four), referred as slave, at the receiver.

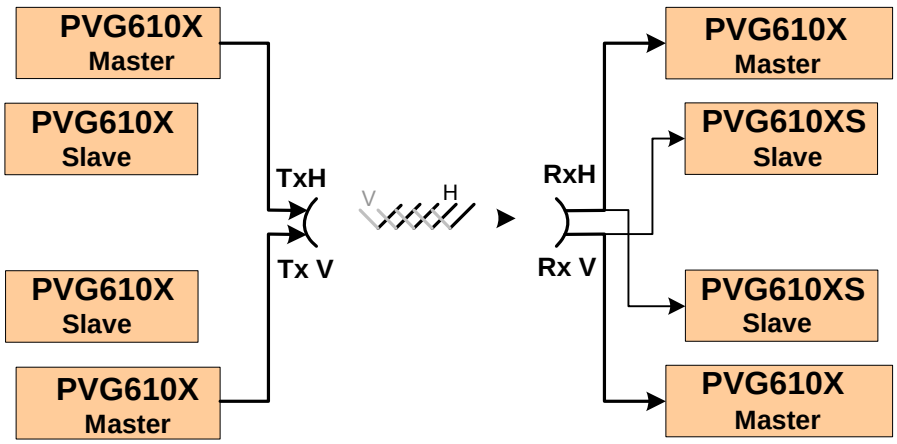


Figure 52: XPIC Master-Slave System Configuration

Crosstalk between the polarizations due to imperfect antenna isolation and channel degradation can be effectively cancelled at the receiver. In order to decode the horizontal channel, the PVG610X Master demodulates the received horizontal signal (which consists of the desired signal and the cross polarity interference). Symbol timing and decision error metrics are passed to the PVG610X Slave chip. The slave demodulates the vertical signal in order to coherently cancel the interference in the horizontal signal. The vertical channel is decoded similarly.

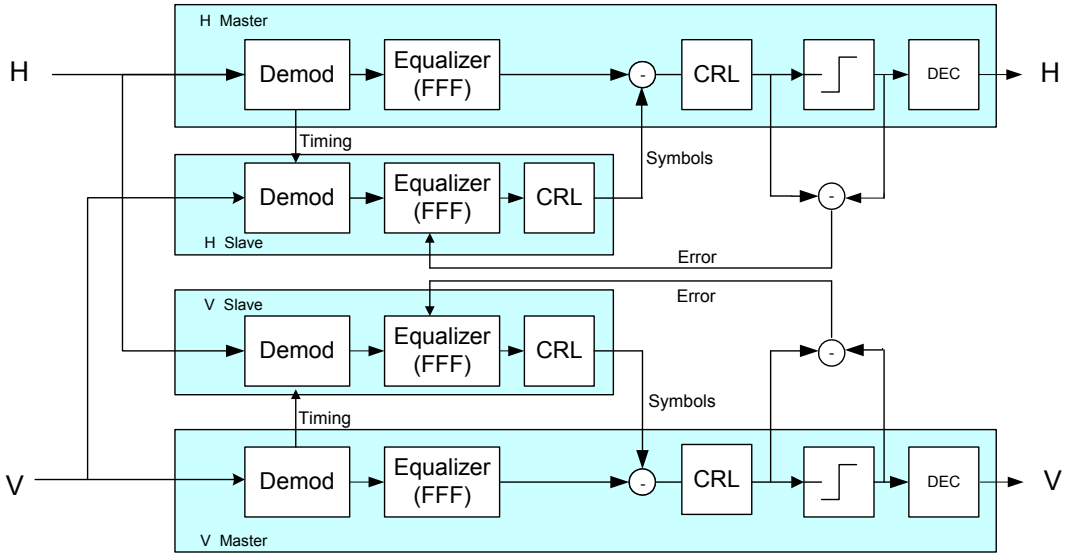


Figure 53: XPIC Interconnection at One End

The above figure describes the interconnections between the four PVG610X at the receiver side of the link. The timing interface between the master and the slave PVG610X ensures coherent timing between sampling in both devices. The symbols interface delivers the sampled data of the opposite channel polarization from the PVG610X Slave to the PVG610X Master. The PVG610X Master subtracts the opposite channel polarization data to cancel the interference, and then delivers the result through the CRL to the slicer.

The error interface channel passes the processed error; the slicer output minus the slicer input to the PVG610X Slave. This processed error is used to adapt the PVG610X equalizer and CRL.

5.3 Boot Modes

PVG610A supports several boot options either from the SPI-FLASH or from the external CPU (SPI-S/DPRAM/UART). The boot options are coded using four boot mode input pins. The mode is set according to the status of these pins during reset. The boot code selects the boot option by reading the boot mode register – bits [3:0] to determine the boot option as described in the following table:

Table 10: Boot Options

	Boot option	Pin [3]	Pin [2]	Pin [1]	Pin [0]
0	External CPU – via parallel Host interface (interleaved mode)	0	0	0	0
1	External CPU – via serial interface (SPI)	0	0	0	1
2	FLASH serial – via SPI	0	0	1	0
3	BOOT Mode for PVG610X Slave	0	0	1	1
4	External CPU – via UART when SYS_CLK = 32.768MHz	0	1	0	0
5	External CPU – via UART when SYS_CLK = 56MHz	0	1	0	1
6	External CPU – via UART when SYS_CLK = 65.536MHz	0	1	1	0
7	External CPU – via UART when SYS_CLK = 80MHz	0	1	1	1
8	External CPU – via UART when SYS_CLK = 93.333MHz	1	0	0	0
9	External CPU – via UART when SYS_CLK = 96MHz	1	0	0	1
10	External CPU – via UART when SYS_CLK = 104MHz	1	0	1	0
11	External CPU – via UART when SYS_CLK = 112MHz	1	0	1	1
12	External CPU – via UART when SYS_CLK = 160MHz	1	1	0	0
13	External CPU – via UART when SYS_CLK = 186.666MHz	1	1	0	1
14	External CPU – via UART when SYS_CLK = 192MHz	1	1	1	0
15	External CPU – via UART when SYS_CLK = 200MHz	1	1	1	1

Notes:

- In XPIC application it is not possible to boot from the Host interface (mode 0 above). In this case, if the boot is performed via external cpu, SPI or UART should be used. After configuration of the device, the external cpu can communicate with the master XPIC device via the host interface (see Figure 88)
- The UART bit rate is 115,200 bps in all cases.

For a detailed description of the Boot process refer to the PVG610A SW Reference Guide.

5.4 System Clock Mode

The system clock can be input to the PVG610A via SYS_CLK pins (LVPECL) or via SPARE_1 pin (LVCMOS).

An internal PLL can be used to multiply or divide the clock signal coming from SYS_CLK or SPARE_1 pins (the PLL can be bypassed if not needed). The multiplication or division factors are rational numbers. The multiplied clock frequency should not exceed 200MHz. Upon power up the PLL is bypassed. The PLL come into action, if required, after running the configuration file.

When using the SPARE_1 pin as the clock source, DFT_TEST pin is set high and DFT[2;0] are set to '010'. In this mode the maximum allowed frequency at the SPARE_1 pin is 100MHz (the clock frequency can then be multiplied by the PLL before feeding the core of the chip).

When using the SYS_CLK pins, DFT_TEST pin is set low and DFT[2;0] pins can be used as GPIO pins. In this mode the maximum allowed frequency at the SYS_CLK pins is 200MHz.

6 Interface Description

This chapter contains information on all active interfaces:

6.1 Pin Sharing Groups

Not all interfaces can operate concurrently. Several interfaces share the same PVG610A pins. The pin assignment depicting the pin sharing is detailed at the beginning of the document. Below is a summary of the shared signals listed according to the interface type.

6.1.1 E1/T1/J1 Interface

Digital E1/T1/J1 signals share pins with analog E1/T1/J1 signals and other signals as listed in the following table:

Table 11: E1/T1/J1 Signals – Pin Sharing Signal List

Digital E1/T1/J1 (Using External LIU)	Analog E1/T1/J1 Signals (Using internal LIU)	Shared Signals
RPOS_[0:20]	RTIP_[0:20]	
RCLK_[0:20]	RRING_[0:20]	
TPOS_[0:20]	TTIP_[0:20]	
TCLK_[0:20]	TRING_[0:20]	
RLOS_[0:15]		HOST_DATA_[0:15]
RLOS_16		HOST_OE
RLOS_17		HOST_WE
RLOS_18		HOST_ADDR_0
RLOS_19		HOST_CS
RLOS_20		HOST_DPRAM_IRQ
MCLK		
ACLK		

6.1.2 MII

MII signals share pins with other signals as follows:

Table 12: MII Signals - Pin Sharing Signal List

MII	Shared Signals
MII_TX_CLK	INJCT2_I_ADC2_A_8
MII_TXD_[0:7]	INJCT2_I_ADC2_A_[0:7], STM1_B_TX_DATA_[0:7]
MII_TX_EN	INJCT2_I_ADC2_A_9, STM1_B_TX_CLK
MII_TX_ER	INJCT2_I_ADC2_A_10, STM1_B_VCXO_PWM
MII_RX_CLK	STM1_B_VCXO_CLK
MII_RXD_[0:7]	INJCT2_Q_ADC2_B_[0:7], STM1_B_RX_DATA_[0:7]
MII_RX_DV	INJCT2_STB_ADC2_CLKIN, STM1_B_RX_CLK
MII_RX_ERR	STM1_B_RX_LOSS
MII_COL	INJCT2_I_ADC2_A_11
MII_CRS	INJCT2_CTRL_4
MII_MDIO	INJCT2_CTRL_0, STM1_B_RX_FP
MII_MDC	INJCT2_Q_ADC2_B_8, STM1_B_RX_SER_CLK

6.1.3 STM-1

STM-1 signals share pins with other signals as follows:

Table 13: STM-1 Signals - Pin Sharing Signal List

STM1	Shared Signals
STM1_REF_CLK	
STM1_A_RX_CLK	
STM1_A_RX_LOSS	
STM1_A_RX_DATA_[0:7]	TX_DATA_[0:7]
STM1_A_TX_CLK	TX_AE
STM1_A_TX_DATA_[0:7]	RX_DATA_[0:7]
STM1_A_VCXO_PWM	
STM1_A_VCXO_CLK	
STM1_B_RX_CLK	MII_RX_DV, INJCT2_STB_ADC2_CLKIN
STM1_B_RX_LOSS	MII_RX_ERR
STM1_B_RX_DATA_[0:7]	MII_RXD_{0:7], INJCT2_Q_ADC2_B_[0:7]
STM1_B_TX_CLK	MII_TX_EN, INJCT2_I_ADC2_A_9
STM1_B_TX_DATA_[0:7]	MII_TXD_[0:7], INJCT2_I_ADC2_A_[0:7]
STM1_B_VCXO_PWM	MII_TX_ER, INJCT2_I_ADC2_A_10
STM1_B_VCXO_CLK	MII_RX_CLK,
TOH Signals	
STM1_A_RX_SER_CLK	DDS1
STM1_A_RX_DATA_OUT	DDS0
STM1_A_RX_DATA_IN	
STM1_A_RX_FP	DDS5
STM1_A_TX_SER_CLK	DDS6
STM1_A_TX_DATA_OUT	DDS2
STM1_A_TX_DATA_IN	DDS_CLK
STM1_A_TX_FP	DDS7
STM1_B_RX_SER_CLK	MII_MDC, INJCT2_Q_ADC2_B_8
STM1_B_RX_DATA_OUT	
STM1_B_RX_DATA_IN	
STM1_B_RX_FP	MII_MDIO, INJCT2_CTRL_0
STM1_B_TX_SER_CLK	INJCT2_CTRL_3
STM1_B_TX_DATA_OUT	
STM1_B_TX_DATA_IN	INJCT2_Q_ADC2_B_10
STM1_B_TX_FP	INJCT2_Q_ADC2_B_11

6.1.4 GPI

GPI signals share pins with other interfaces as follows:

Table 14: GPI Signals - Pin Sharing Signal List

Injection Bus	Shared Signals
DDS0	STM1_A_RX_DATA_OUT
DDS1	STM1_A_RX_SER_CLK
DDS2	STM1_A_TX_DATA_OUT
DDS3	
DDS4	
DDS5	STM1_A_RX_FP
DDS6	STM1-A_TXSER_CLK
DDS7	STM1_A_TX_FP
DDS_CLK	STM1_A_TX_DATA_IN
RX_CLK	
RX_DATA_[0:7]	STM1_A_TX_DATA_[0:7]
RX_RE	
RX_AF	
RX_AE	
RX_SYNC	
RX_ACM	
RX_UNCOR	
TX_CLK	
TX_DATA_[0:7]	STM1_A_RX_DATA_[0:7]
TX_WE	
TX_AF	
TX_AE	STM1_A_TX_CLK
TX_SYNC	
TX_ACM	

6.1.5 Host Interface

Host Interface signals share pins with other signals as follows:

Table 15: Host Signals - Pin Sharing Signal List

Host Interface	Shared Signals
HOST_ADDR_0	RLOS_18
HOST_ADDR_[1:4]	SDRAM_DATA_[12:15]
HOST_ADDR_[5:6]	SDRAM_DQMOUT_[0:1]
HOST_ADDR_[7:9]	SDRAM_ADDROUT_[12:14]
HOST_ADDR_10	INJCT2_CTRL_1
HOST_ADDR_11	INJCT2_CTRL_2
HOST_ADDR_[12:15]	GPIO_[4:7], SPI_M_CS_[4:7]
HOST_DATA_[0:15]	RLOS_[0:15]
HOST_OE	RLOS_16
HOST_WE	RLOS_17
HOST_CS	RLOS_19
HOST_DPRAM_IRQ	RLOS_20
HOST_INT	
XPIC_HOST_CS_N	

6.1.6 SPI

SPI master and slave interfaces share pins with each other and with other interfaces as follows:

Table 16: SPI Signals - Pin Sharing Signal List

SPI Master	SPI Slave	Shared Signals
SPI_M2_CS_0		DC_COR_I
SPI_M2_DO		DC_COR_Q
SPI_M2_DI		DC_COR_EN
SPI_M2_CLK		DC_COR_CLK
SPI_M_CS_0	SPI_S_CS	
SPI_M_CLK	SPI_S_CLK	
SPI_M_DI	SPI_S_DI	
SPI_M_DO	SPI_S_DO	
SPI_M_CS_[1:3]		GPIO_[13:15]
SPI_M_CS_[4:7]		GPIO_[4:7], HOST_ADDR_[12:15]

6.1.7 OMI & HDLC Interfaces

OMI share signals with HDLC interface follows:

Table 17: OMI and HDLC Pin Sharing

OMI	HDLC
OMI_TCLK	HDLC_TCLK
OMI_TXD	HDLC_TXD
OMI_RCLK	HDLC_RCLK
OMI_RXD	HDLC_RXD

6.1.8 DC Correction

DC Correction signals are shared with SPI signals as follows:

Table 18: DC Correction and SPI Pin Sharing

DC Correction	Shared Signals
DC_COR_I	SPI_M2_CS_0
DC_COR_Q	SPI_M2_DO
DC_COR_EN	SPI_M2_DI
DC_COR_CLK	SPI_M2_CLK

6.1.9 Protection

Two protection signals share pins with GPIO pins as listed in the table. The rest of the protection pins are unshared.

Table 19: Protection and GPIO Pin Sharing

Protection	Shared Signals
TXP_CLKOUT	GPIO_10
RXP_CLKOUT	GPIO_12

6.1.10 SDRAM

SDRAM signals share pins with other signals as follows:

Table 20: SDRAM Signals - Pin Sharing Signal List

SDRAM	Shared Signals
SDRAM_ADDROUT_[0:11]	INJCT_Q_ADC_B_[0:11], DAC_Q_[0:11]
SDRAM_ADDROUT_[12:14]	HOST_ADDR_[7:9]
SDRAM_DATA_[0:11]	INJCT_I_ADC_A_[0:11], DAC_I_[0:11]
SDRAM_DATA_[12:15]	HOST_ADDR_[1:4]
SDRAM_N_RASOUT	INJCT_CTRL_0
SDRAM_N_CASOUT	INJCT_STB_ADC_CLKIN
SDRAM_CLKOUT	INJCT_CTRL_3
SDRAM_N_DYCSOUT	INJCT_CTRL_1
SDRAM_N_WEOUT	INJCT_CTRL_2
SDRAM_FBCLKIN	INJCT_CTRL_4
SDRAM_DQMOUT_[0:1]	HOST_ADDR_[5:6]

6.1.11 GPIO

GPIO signals share pins with other signals as follows:

Table 21: GPIO Signals - Pin Sharing Signal List

GPIO	Shared Signals
GPIO_[0:2]	DFT_[0:2]
GPIO_3	
GPIO_[4:7]	HOST_ADDR_[12:15], SPI_M_CS_[4:7]
GPIO_8	EVENT_PHY_IRQ
GPIO_9	ALARM_RX_NET_IRQ
GPIO_10	TXP_CLKOUT
GPIO_11	ALARM_TX_NET_IRQ
GPIO_12	RXP_CLKOUT
GPIO_[13:15]	SPI_M_CS_[1:3]

6.1.12 Injection Bus, External ADC/DAC

Injection Bus 1, used for external ADC and DAC connections, shares pins with SDRAM interface. Injection Bus 2 shares pins with other interfaces. The sharing information is summarized in the table.

Table 22: Injection Bus, ADC/DAC Signals - Pin Sharing Signal List

Injection Bus / External ADC/DAC	Shared Signals
INJCT_I_ADC_A_[0:11], DAC_I_[0:11]	SDRAM_DATA_[0:11]
INJCT_Q_ADC_B_[0:11], DAC_Q_[0:11]	SDRAM_ADDROUT_[0:11]
INJCT_CTRL_0	SDRAM_N_RASOUT
INJCT_CTRL_1	SDRAM_N_DYCSOUT
INJCT_CTRL_2	SDRAM_N_WEOUT
INJCT_CTRL_3	SDRAM_CLKOUT
INJCT_CTRL_4	SDRAM_FBCLKIN
INJCT_STB_ADC_CLKIN	SDRAM_N_CASOUT
INJCT2_I_ADC2_A_[0:7]	MII_TXD_[0:7], STM1_B_TX_DATA_[0:7]
INJCT2_I_ADC2_A_8	MII_TX_CLK
INJCT2_I_ADC2_A_9	MII_TX_EN, STM1_B_TX_CLK
INJCT2_I_ADC2_A_10	MII_TX_ER, STM1_B_VCXO_PWM
INJCT2_I_ADC2_A_11	MII_COL
INJCT2_Q_ADC2_B_[0:7]	MII_RXD_[0:7], STM1_B_RX_DATA_[0:7]
INJCT2_Q_ADC2_B_8	MII_MDC, STM1_B_RX_SER_CLK
INJCT2_Q_ADC2_B_10	STM1_B_TX_DATA_IN
INJCT2_Q_ADC2_B_11	STM1_B_TX_FP
INJCT2_CTRL_0	MII_MDIO, STM1_B_RX_FP
INJCT2_CTRL_1	HOST_ADDR_10
INJCT2_CTRL_2	HOST_ADDR_11
INJCT2_CTRL_3	STM1_B_TX_SER_CLK
INJCT2_CTRL_4	MII_CRS
INJCT2_STB_ADC2_CLKIN	MII_RX_DV, STM1_B_RX_CLK

6.2 Data Interfaces

6.2.1 E1/T1/J1 with Integrated LIU

The PVG610A contains 21 E1/T1J1 integrated LIU's (of which one is dedicated for temperature calibration circuit and 20 are available for transfer of user data). The following figure illustrates the E1/T1/J1 lines interfacing with the PVG610, using its integrated LIU.

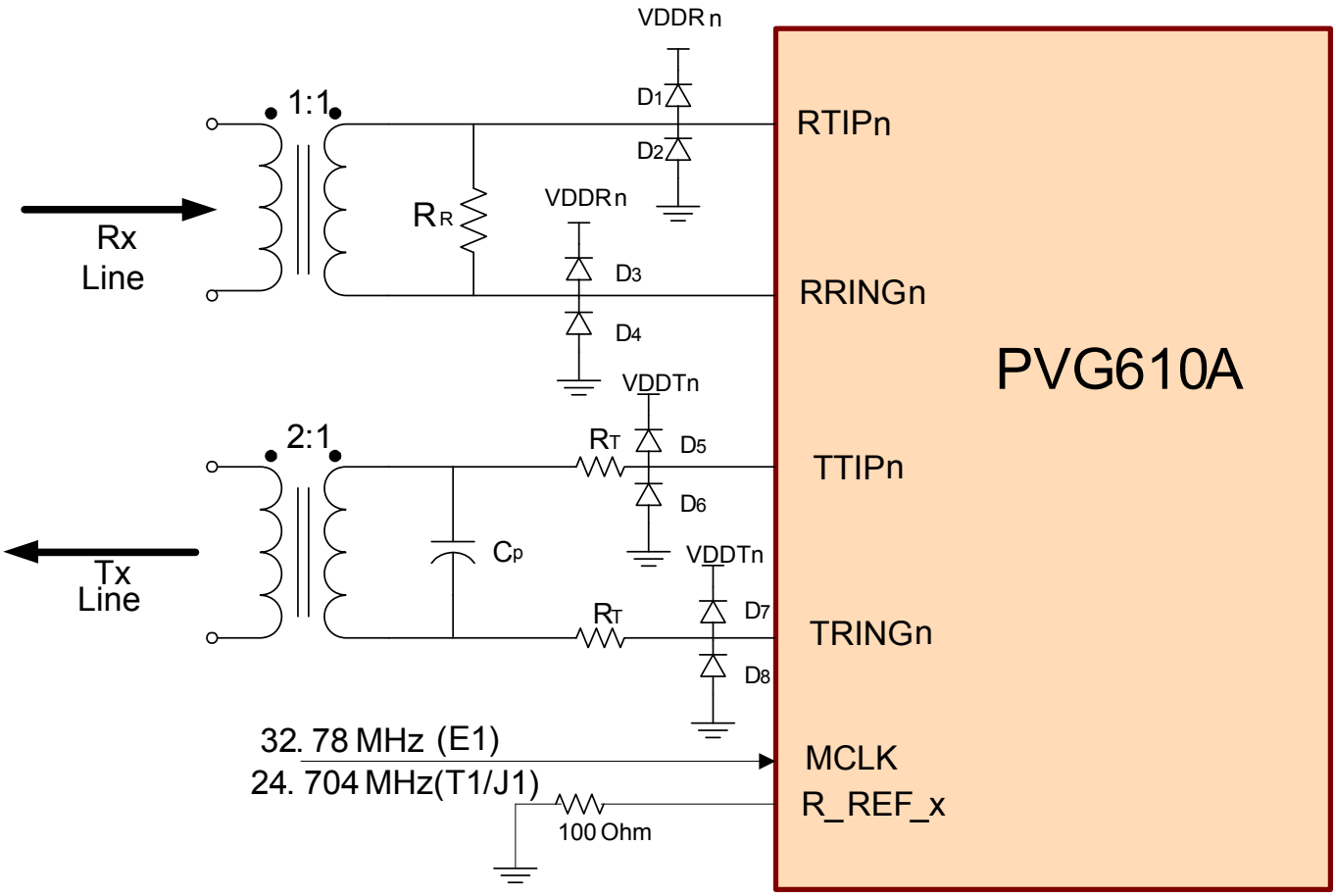


Figure 54: E1/T1/J1 Connection Diagram

The integrated LIU contains internal impedance matching circuits supporting multiple line types without having to change external components. The supported line types are 100 Ω/T1, 110 Ω/J1 twisted pair, 120 Ω/E1 twisted pair and 75 Ω/ E1 coax.

A 1:1 transformer is to be used in the receive path and a 1:2 transformer in the transmit path.

All E1/T1/J1 links share a single clock line; 32.768 MHz for E1 or 24.704 MHz for or T1/J1.

A 100ohm resistor (±1%) has to be connected between each of the three R_REF_xx pins at the PVG610A and ground. For unused E1/T1/J1 links the corresponding R_REF_x pins may remain unconnected.

R_REF_0 is used for links 0-3

R_REF_12 is used for links 4-16

R_REF_17 is used for links 17-20.

For detailed description of the peripheral circuitry refer to the PVG610A LIU application note.

6.2.1.1 Receiver Characteristics

Table 23: Receiver Characteristics for E1 Links

Symbol	Parameter	Min	Typ	Max	Units	Test conditions/Remark
	Receiver sensitivity - Short haul with cable loss @1024kHz			-10	dB	Up to 0.67V for 75Ω Up to 0.85V for 120Ω
	Analog LOS - Short haul		800		mVp-p	
	Allowable consecutive zeroes before LOS: - G.775 - I.431 / ETSI300233		32 2048			
	LOS reset	12.5			%	G.775, ETSI300233 12.5% for M consecutive pulse intervals
ZDM	Receiver differential input impedance	10			kΩ	Internal mode
	Input termination resistor tolerance			+/- 1%		
RRX	Receive Return Loss (G.703) 51 KHz – 102 KHz 102 KHz – 2.048 MHz 2.048 MHz – 3.072 MHz		 26 26 26		 dB dB dB	Note: the return loss is for the complete system (including the transformer).

Table 24: Receiver characteristics for T1/J1 links

Symbol	Parameter	Min	Typ	Max	Units	Test conditions
	Receiver sensitivity - Short haul with cable loss @772kHz			-10	dB	Up to 0.76V
	Analog LOS - Short haul		800		mVp-p	
	Allowable consecutive zeroes before LOS: - G.775 - I.431		175 1544			
	LOS reset	12.5			%	G.775, ETSI300233 12.5% for M consecutive pulse intervals
ZDM	Receiver differential input impedance	20			kΩ	Internal mode
	Input termination resistor tolerance			+/- 1%		
RRX	Receive Return Loss (G.703) 39 KHz – 77 KHz 77 KHz – 1.544 MHz 1.544 MHz – 2.316 MHz		 26 26 26		 dB dB dB	Note: The return loss is for the complete system (including the transformer).

Table 25: LOS detection and clear levels

		Standard		
		ANSI T1.231 for T1	**G.775 for E1**	**ETSI 300233 for E1**
LOS Detected	Continuous Intervals	175	32	2048(1ms)
	Amplitude	Below typ. 310mv (Vpp)	Below typ. 310mv (Vpp)	Below typ. 310mv (Vpp)
LOS Cleared	Density	12.5% (16 marks in a sliding 128-bit period) with no more than 99 continuous zeros.	12.5% (4 marks in a sliding 32-bit period) with no more than 15 continuous zeros.	12.5% (4 marks in a sliding 32-bit period) with no more that 15 continuous zeros.
	Amplitude	Exceed typ. 540mv (Vpp)	Exceed typ. 540mv (Vpp)	Exceed typ. 540mv (Vpp)

6.2.1.2 Transmitter Characteristics

Pulse Shape:

The shape of the pulses changes according to the link type to ensure that the T1/E1 pulse maintains compliance with the required template after the signal has passed through different cable lengths or types. The following link types and cable length are supported:

- E1/75 Ω
- E1/120 Ω,
- T1/ 100 Ω / 0-133 ft
- J1/ 110 Ω / 0-133 ft

For E1 applications, the pulse shape is according to the G.703 standard as shown in the following figures.

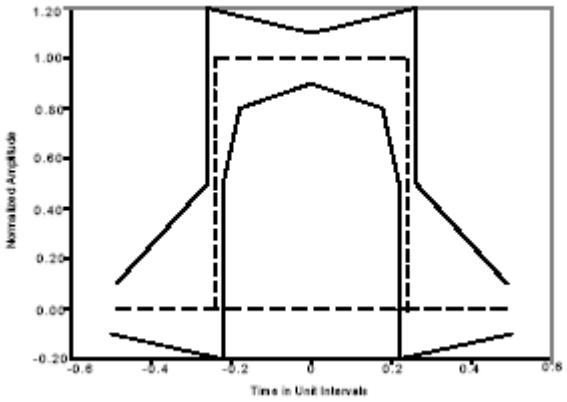
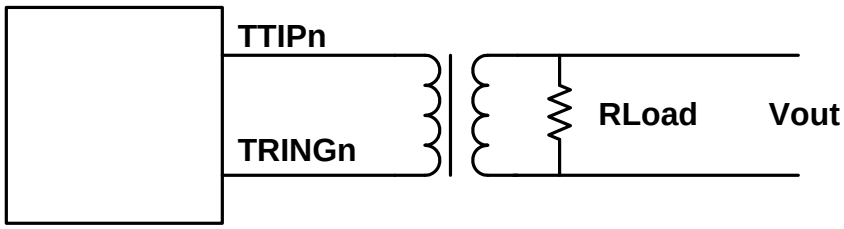


Figure 55: E1 Waveform Template Diagram



Note: For RLoad=75 Ohm (nom), Vout(peak)=2.37 V (nom)
For RLoad=120 Ohm (nom), Vout(peak)=3.00 V (nom)

Figure 56: E1 Pulse Template Test Circuit

For T1 applications, the pulse shape is shown below and is according to the T1.102 specification (it also meets the requirement of G.703, 2001).

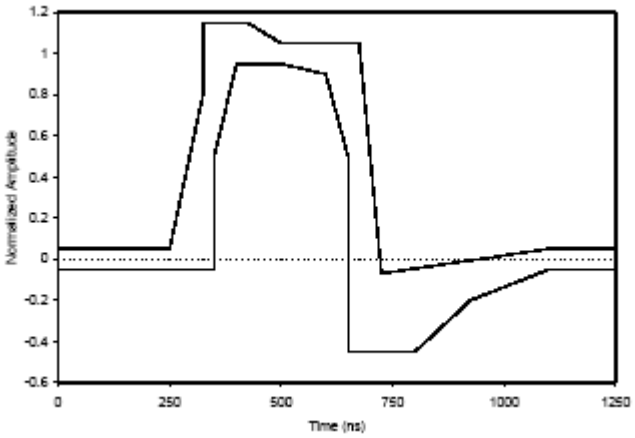
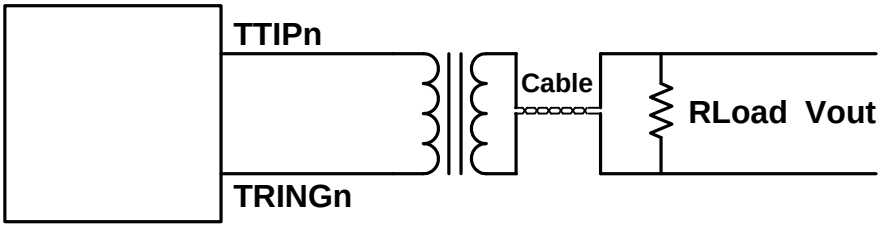


Figure 57: T1 Waveform Template Diagram

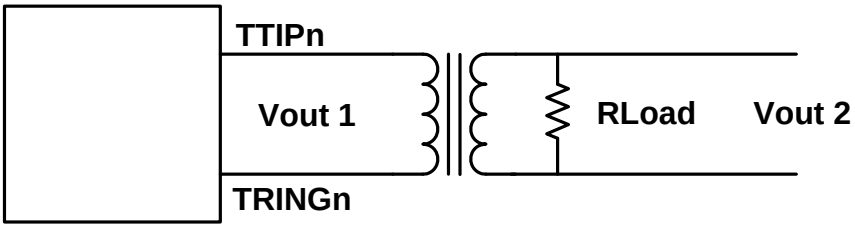


RLoad =100 ohm +/-5%

Figure 58: T1 Pulse Template Test Circuit

Line Driver:

The tables below specify the Line Driver characteristics for E1 and T1 links. The figure illustrates the references for the specification tables.



RLoad=75 Ohm (nom), Vout 2 (peak)=2.37 V (nom)
RLoad=120 Ohm (nom), Vout 2 (peak)=3.00 V (nom)

Figure 59: Transmit Line Circuit

Table 26: Line Driver characteristics for E1 links:

Symbol	Parameter	Min	Typ	Max	Units
Vo-p (Vout 1)	Line driver Output pulse amplitudes E1, 75 Ω load E1, 120 Ω load	 1.07 1.35	 1.18 1.5	 1.3 1.65	 V V
Vo-p (Vout 1)	Zero (space) level E1, 75 Ω load E1, 120 Ω load	 -0.119 -0.15	 	 0.119 0.15	 V V
Vo-p (Vout 2)	Output pulse amplitudes E1, 75 Ω load E1, 120 Ω load	 2.14 2.7	 2.37 3.0	 2.60 3.3	 V V
Vo-p (Vout 2)	Zero (space) level E1, 75 Ω load E1, 120 Ω load	 -0.237 -0.3	 	 0.237 0.3	 V V
	Transmit amplitude variation with supply	-1		-1	%
	Difference between pulse sequences for 17 consecutive pulses (T1.102)			200	mV
Tpw	Output Pulse Width at 50% of nominal amplitude	232	244	256	ns
	Ratio of the amplitude of positive and negative pulses at the center of the pulse interval (G.703)	0.95		1.05	
	Ratio of the width of positive and negative pulses at the center of the pulse interval (G.703)	0.95		1.05	
RTX	Transmit Return Loss (G.703) 51 KHz – 102 KHz 102 KHz – 2.048 MHz 2.048 MHz – 3.072 MHz Note: this return loss is for the complete system (including the transformer).		20 15 12		dB dB dB
Isc	Line short circuit current		100		mA I p-p

Table 27: Line Driver characteristics for T1/J1 links:

Symbol	Parameter	Min	Typ	Max	Units
Vo-p (Vout 1)	Output pulse amplitude	1.2	1.5	1.8	V
Vo-p (Vout 1)	Zero (space) level	-0.08		0.08	V
Vo-p (Vout 2)	Output pulse amplitude	2.4	3.0	3.6	V
Vo-p (Vout 2)	Zero (space) level	-0.15		0.15	V
	Transmit amplitude variation with supply	-1		-1	%
	Difference between pulse sequences for 17 consecutive pulses (T1.102)			200	mV
Tpw	Output Pulse Width at 50% of nominal amplitude	338	350	362	ns
	Imbalance between positive and negative pulses amplitude (T1.102)	0.95		1.05	
	Pulse width variation of half amplitude (T1.102)			20	ns
	Output power level @772 kHz @1544 kHz (referenced to power at 772 kHz)	 12.6 -29		 17.9	 dBm dB
RTX	Transmit Return Loss (G.703) 39 KHz – 77 KHz 77 KHz – 1.544 MHz 1.544 MHz – 2.316 MHz Note: this return loss is for the complete system (including the transformer).		 20 15 12		 dB dB dB
Isc	Line short circuit current		100		mA I p-p

6.2.2 E1/T1/J1 Connection with External LIU

The following figure illustrates the E1/T1/J1 lines connecting to the PVG610, using an external LIU.

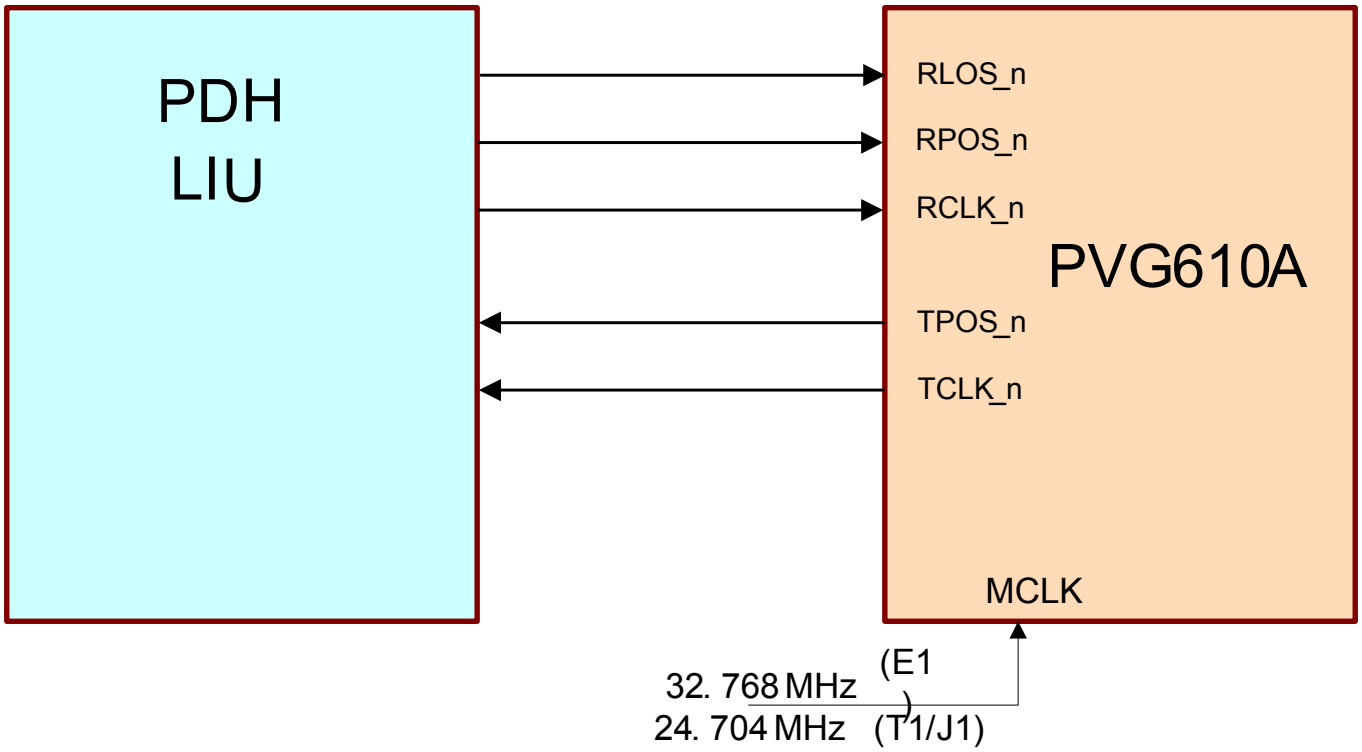


Figure 60: E1/T1/J1 Connections Diagram – External LIU

RCLK and TCLK are used to sample data in or out the PVG610A (their frequency is identical to the payload rate). RLOS signal is asserted when LOS is detected by the LIU.

6.2.2.1 AC Characteristics

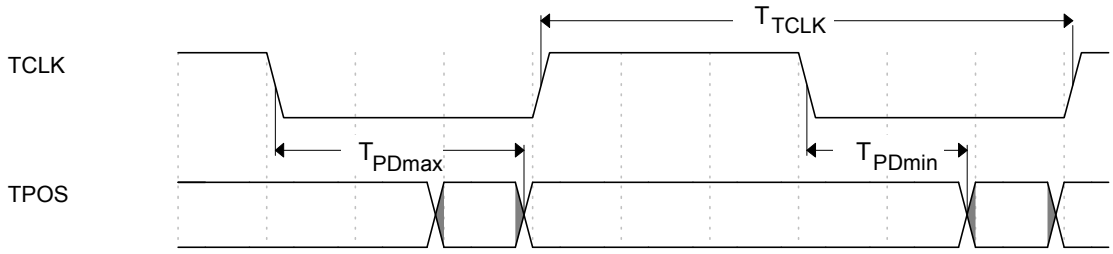


Figure 61: Transmit Timing Diagram

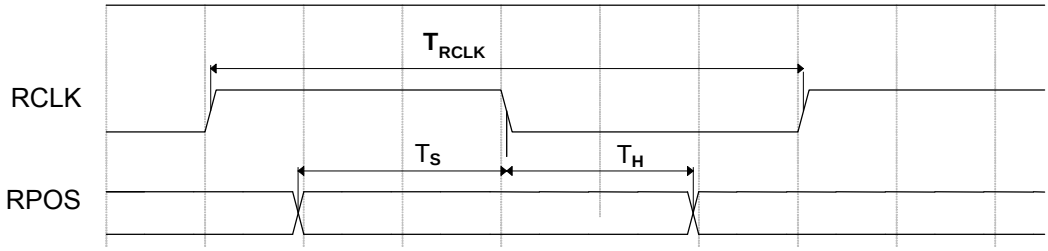


Figure 62: Receive Timing Diagram

Table 28: E1/T1/J1 AC Characteristics

Parameter	Symbol	Min	Max	Units
Transmit				
Transmit clock period	T_{TCLK}	488		ns
Transmit TCLK to TPOS Propagation delay	T_{PD}	245	250	ns
Rise time*			55	Ns
Fall time*			35	ns
Receive				
Receive clock period	T_{RCLK}	488		ns
RPOS to RCLK falling edge set up time	T_S	10		ns
RCLK falling edge to RPOS hold time	T_H	10		ns

* Rise/fall time is specified for 15pf load

6.2.3 Ethernet I/F - MII, GMII

An Ethernet PHY can be directly connected to the PVG610. Two types of interfaces are supported:

- MII – supporting 10Mbps and 100 Mbps
- GMII – supporting 1000 Mbps

In all cases a two-line management interface is used to manage the Ethernet PHY.
All interfaces are compliant to the IEEE 802.3 standard.

6.2.3.1 MII Management Interface (MDC/MDIO)

This interface has two lines:

- MII_MDC – Clock signal (from PVG610A to the Ethernet PHY)
- MII_MDIO – Bidirectional data line

6.2.3.2 AC Characteristics

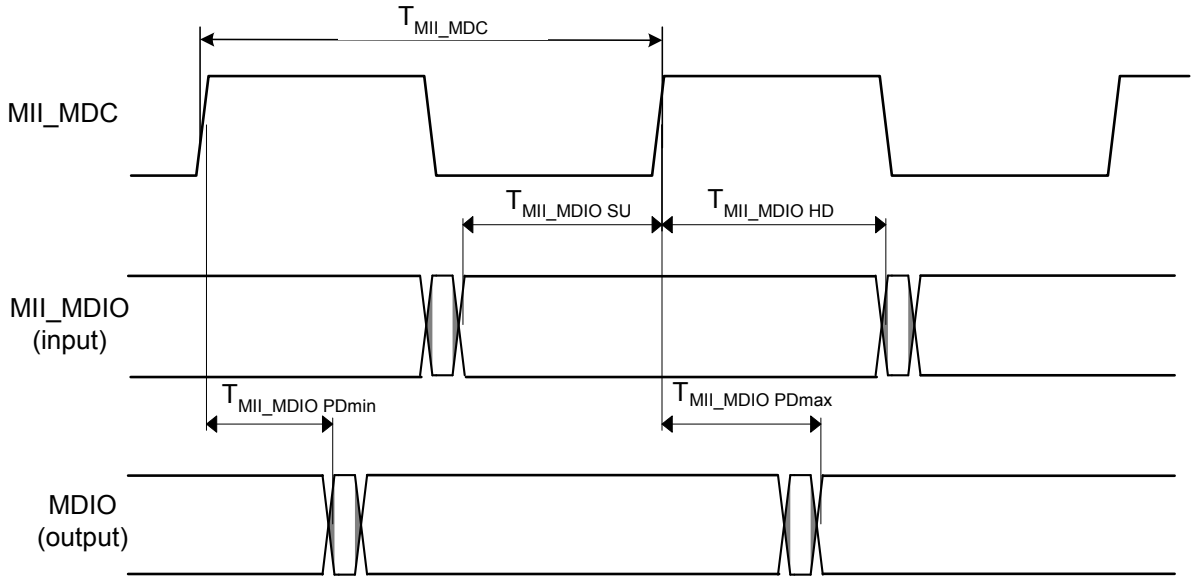


Figure 63: MDC/MDIO Timing Diagram

Table 29: MII AC Characteristics

Parameter	Symbol	Min	Max	Units
MII_MDC period	TMII_MDC	80		ns
MII_MDIO(input) to MDC Set up time	TMII_MDIO SU	10		ns
MII_MDIO(input) to MDC Hold time	TMII_MDIO HD	10		ns
MDC to MDIO (output) propagation delay	TMII_MDIO PD	2*SYS_CLK_CYCLE - 3	2*SYS_CLK_CYCLE	ns

6.2.3.3 MII Interface

The MII interface is used to transfer Ethernet data of 10 Mbps and 100 Mbps modes. The following figure illustrates the connection between an Ethernet PHY and the PVG610A using MII signals.

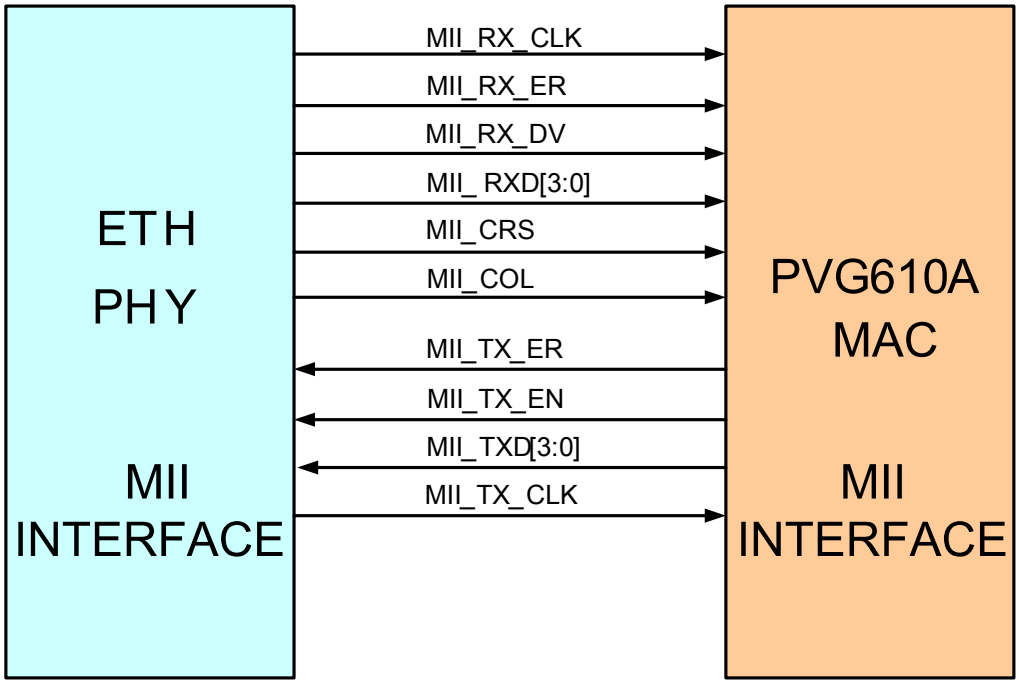


Figure 64: MII interface Lines

The clock signals are sourced by the Ethernet PHY. The clock frequency is 2.5 MHz for the 10 Mbps mode and 25 MHz for the 100 Mbps mode.

6.2.3.4 AC Characteristics

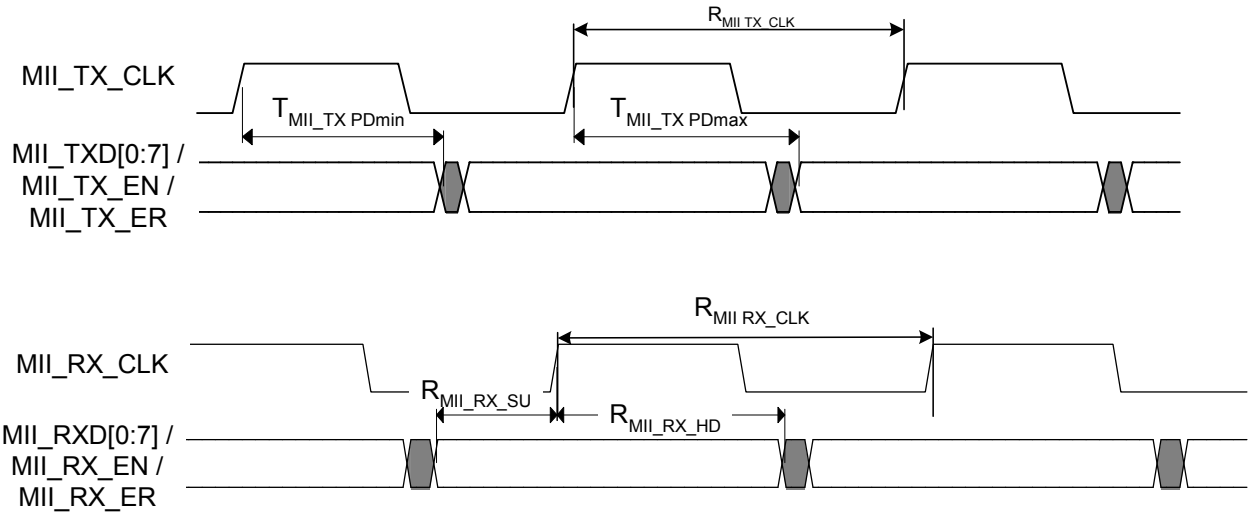


Figure 65: MII Timing Diagrams

Table 30: 10Base Timing

Parameter	Symbol	Min	Max	Units	Remarks
MII_TX _CLK cycle time	TMII TX_CLK	400		ns	
MII_TXD[0:7]/ MII_TX_EN/ MII_TX_ER propagation delay in reference to MII_TX _CLK clock	TMII_TX PD	3.3	8.56	ns	
MII_RX_CLK cycle time	RMII RX_CLK	400		ns	
MII_RXD[0:7]/ MII_RX_DV/ MII_RX_ER Set up time in relation to MII_RX_CLK clock	RMII_RX_SU	-0.8		ns	
MII_RXD[0:7]/ MII_RX_DV/ MII_RX_ER Hold time in relation to MII_RX_CLK clock	RMII_RX_HD	4.3		ns	

Table 31: 100Base Timing

Parameter	Symbol	Min	Max	Units	Remarks
MII_TX _CLK cycle time	TMII TX_CLK	40		ns	
MII_TXD[0:7]/ MII_TX_EN/ MII_TX_ER propagation delay in respect to MII_TX _CLK clock	TMII_TX PD	3.3	8.56	ns	
MII_RX_CLK cycle time	RMII RX_CLK	40		ns	
MII_RXD[0:7]/ MII_RX_DV/ MII_RX_ER Set up time in respect to MII_RX_CLK clock	RMII_RX_SU	-0.8		ns	
MII_RXD[0:7]/ MII_RX_DV/ MII_RX_ER Hold time in respect to MII_RX_CLK clock	RMII_RX_HD	4.3		ns	

6.2.3.5 GMII

GMII interface is used to transfer Ethernet data for 1000 Mbps mode. The following figure illustrates the connection of an Ethernet PHY to the PVG610A using the GMII signals.

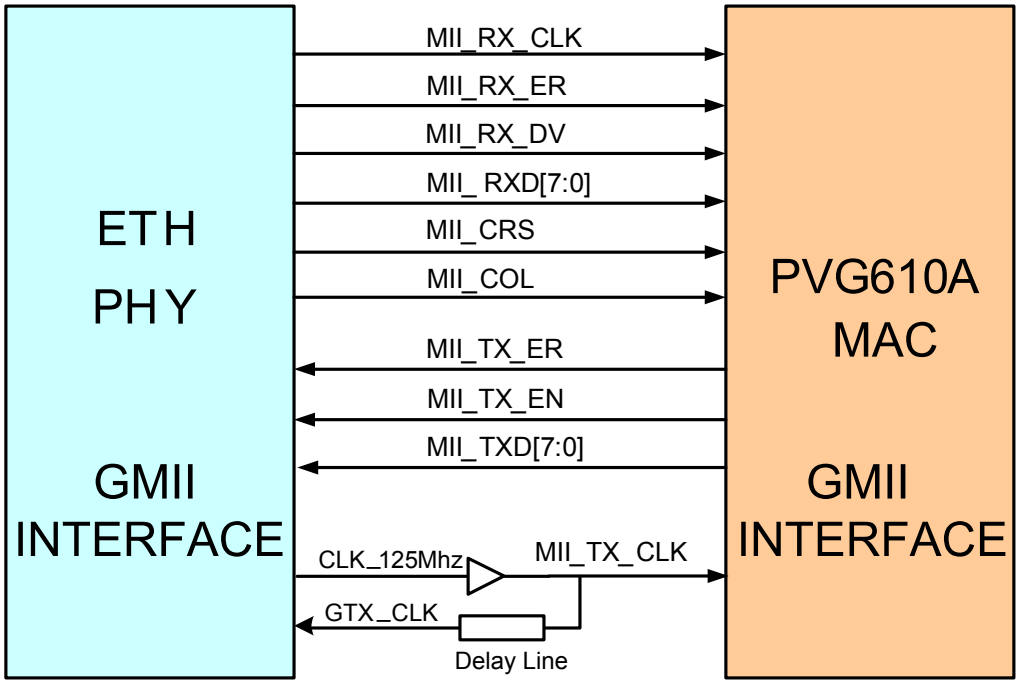


Figure 66: GMII interface Lines

The clock signals are sourced by the Ethernet PHY. The clock frequency is 125 MHz.
When working with GMII interface the system's clock rate should be higher than 125MHz.

6.2.3.6 AC Characteristics

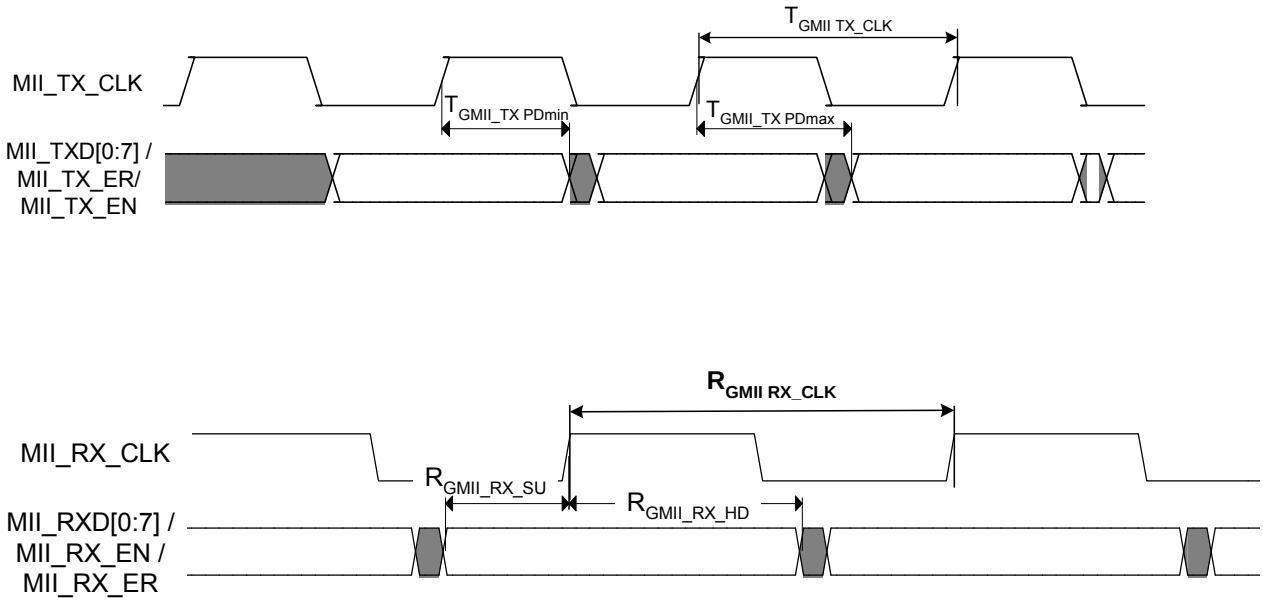


Figure 67: GMII Timing Diagrams

Table 32: GMII AC Characteristics

Parameter	Symbol	Min	Max	Units	Remarks
MII_TX _CLK cycle time	TGMII TX_CLK	8		ns	
MII_TXD[0:7]/ MII_TX_EN/ MII_TX_ER propagation delay in respect to MII_TX _CLK clock	TGMII_TX PD	3.3	8.56	ns	
MII_RX_CLK cycle time	RGMII RX_CLK	8		ns	
MII_RXD[0:7]/ MII_RX_DV/ MII_RX_ER Set up time in respect to MII_RX_CLK clock	RGMII_RX_SU	-0.8		ns	
MII_RXD[0:7]/ MII_RX_DV/ MII_RX_ER Hold time in respect to MII_RX_CLK clock	RGMII_RX_HD	4.3		ns	

6.2.4 STM-1

The PVG610A supports the transport of two STM-1/OC-3 links (denoted as STM1-A and STM1-B). The STM-1 interface allows the connection of STM-1/OC-3 SERDES to the PVG610. The following figure illustrates the connection of the SERDES to the PVG610.

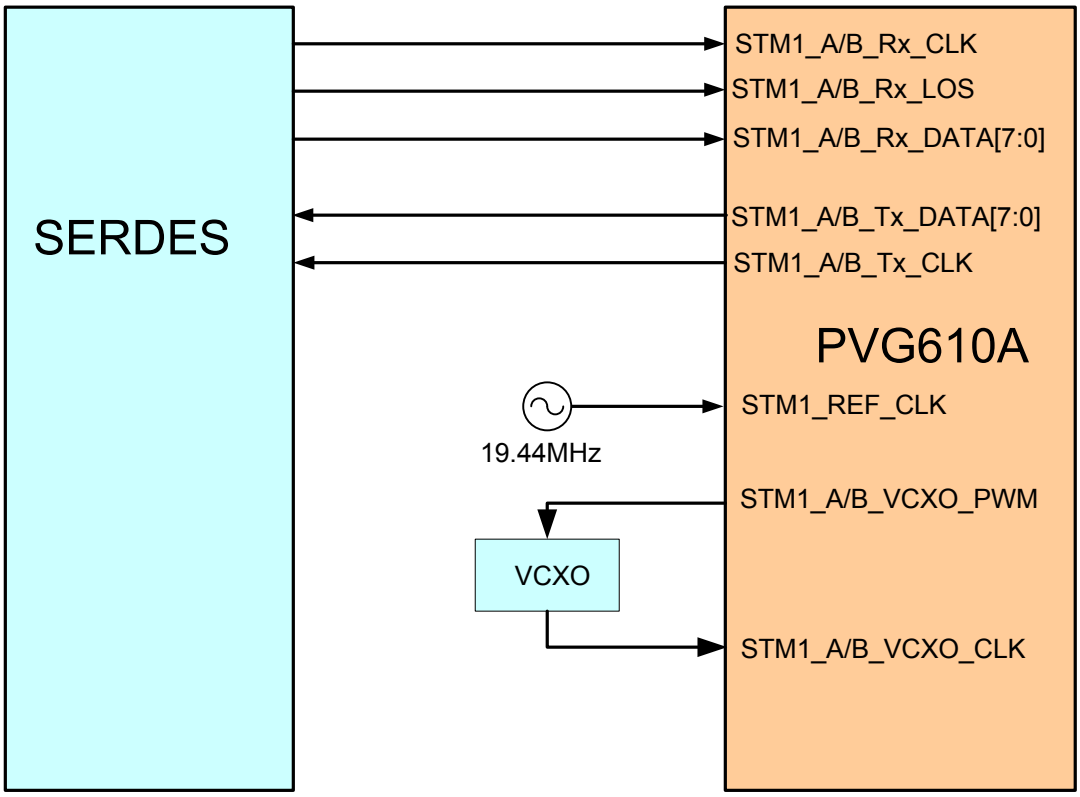


Figure 68: STM1 Connection Diagram

Note the following:

- RX_CLK and TX_CLK signals run at 19.44 MHz and are used to sample RX/TX data in or out the PVG610.
- LOS signal is asserted when the SERDES identifies Los of Signal.
- The VCXO is used by the PVG610A to reconstruct the TX clock from the data stream coming from the radio.
- The 19.44MHz clock (STM1_REF_CLK) is shared by both links. This clock is used by the PVG610A to maintain a data stream toward the SERDES (TX direction) when the air link is inactive and to maintain a data stream toward the air (RX direction) when in an LOS events at the line side.

6.2.4.1 AC Characteristics

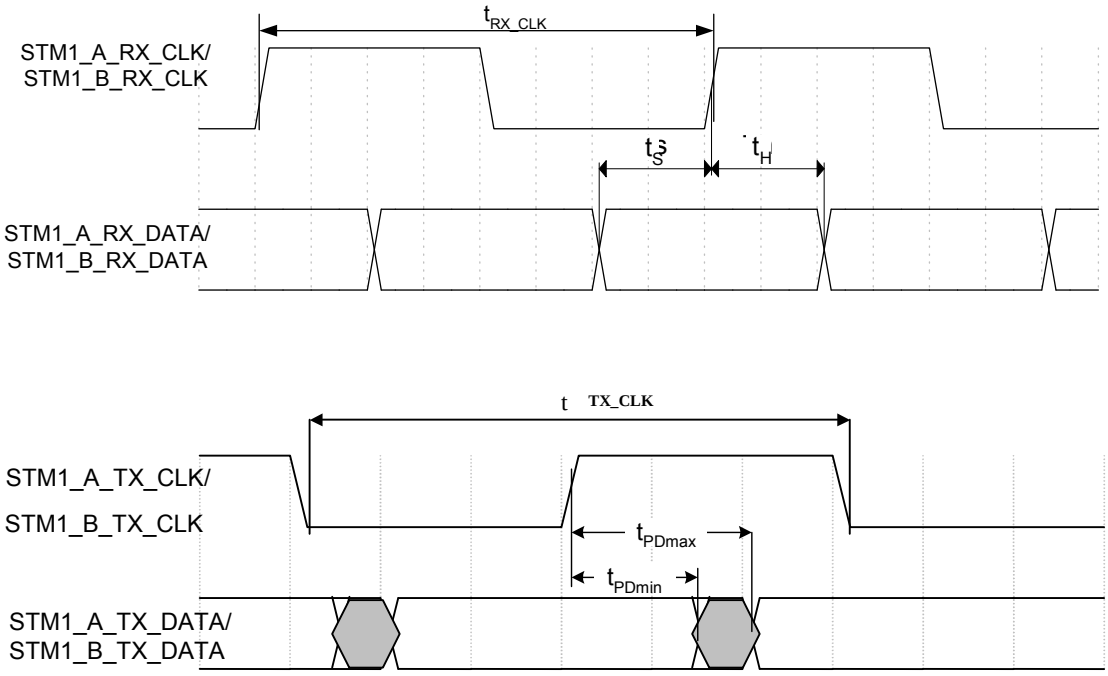


Figure 69: STM-1 Timing Diagram

Table 33: STM-1 AC Characteristics

Parameter	Symbol	Min	Max	Units
Transmit				
STM1_B_TX_CLK clock period	t_{RX_CLK}		51.44	ns
STM1_B_TX_CLK to STM1_B_TX_DATA propagation delay	t_{PD}	5.7	13	ns
Receive				
Receive clock period			51.44	ns
STM1_B_RX_DATA to STM1_B_RX_CLK setup time	t_S	1.5		ns
STM1_B_RX_CLK to STM1_B_RX_DATA hold time	t_H	1.15		ns

6.2.5 TOH

The TOH interface is used to extract/insert TOH data from/to the STM-1 streams. There are two TOH interfaces, each for one of the two STM-1 links (i.e. A and B). Each TOH interface is comprised of two groups:

- RX: data is extracted from the line STM-1 stream and inserted into the radio STM-1 stream. .
- TX: data is extracted from the radio STM-1 stream and inserted into the line STM-1 stream.

The TOH interfaces can be configured to extract/insert general TOH data, Section DCC or Line DCC. When configured to transfer general TOH data, the PVG610A enables extracting the entire TOH field and inserting parts (or all) of the TOH field in granularity of 64kbps. Note that the RX TOH lines can be configured to work in a different mode compared to the TX TOH lines (for example the RX TOH lines can transfer Section DCC while the TX TOH can transfer Line DCC).

The following figure depicts the TOH interface lines.

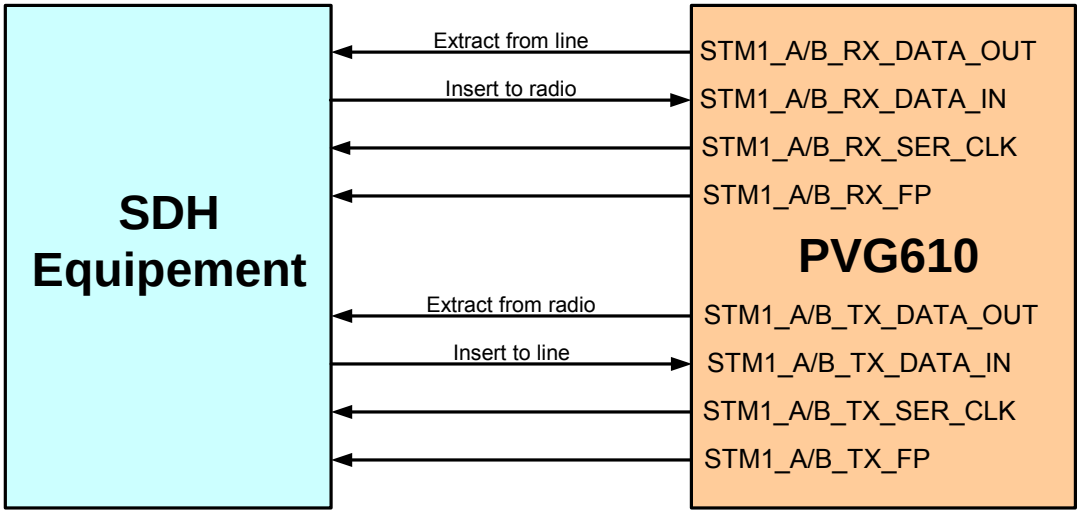


Figure 70: TOH Interface

Data is sampled in and out the PVG610A at every rising clock.

The clock frequency used to extract TOH is in the range of 5.26 – 5.6MHz (depending on the configured system clock). It has a 50% duty cycle. The clock has silence periods following each stream of 9 bytes (the number of bytes in one SDH/SONET line).

The Frame Pulse (FP) signal marks the start of an STM-1 frame (the first TOH bit arrives one clock after FP).

The following figure depicts the interface-protocol in this mode

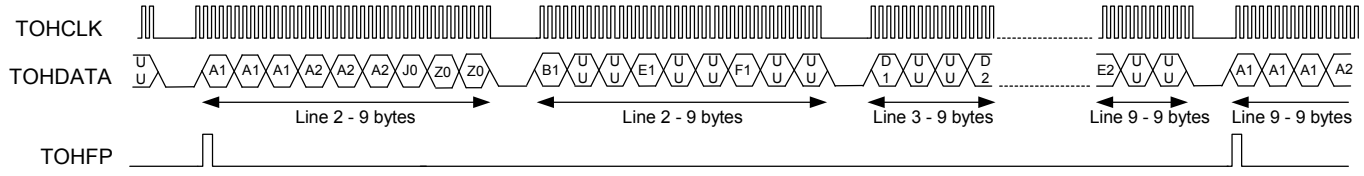


Figure 71: TOH Extract Interface-Protocol

The clock frequency used for the DCC section is in the range of 192.6-193.5 KHz (depending on the system clock). The clock has a silence period between consecutive frames (as shown in the following figure).

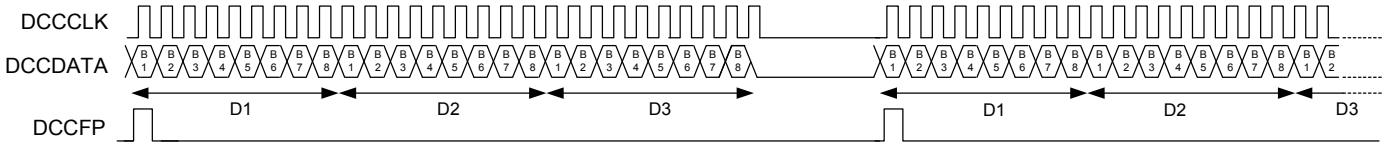


Figure 72: Section DCC Extract Interface-Protocol

The clock frequency used for Line DCC is in the range of 581.3-589.1 KHz (depending on the system clock). The clock has a silence period between consecutive frames (as shown in the following figure).

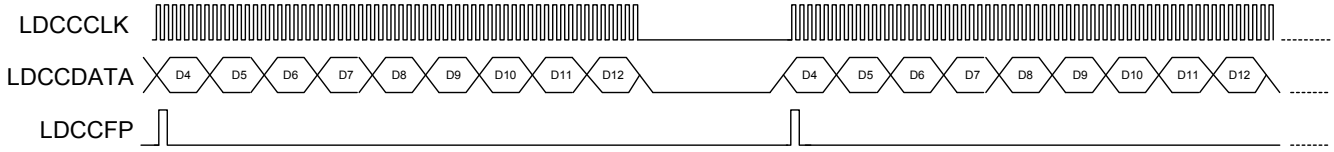


Figure 73: Line DCC Extract Interface-Protocol

6.2.5.1 AC Characteristics

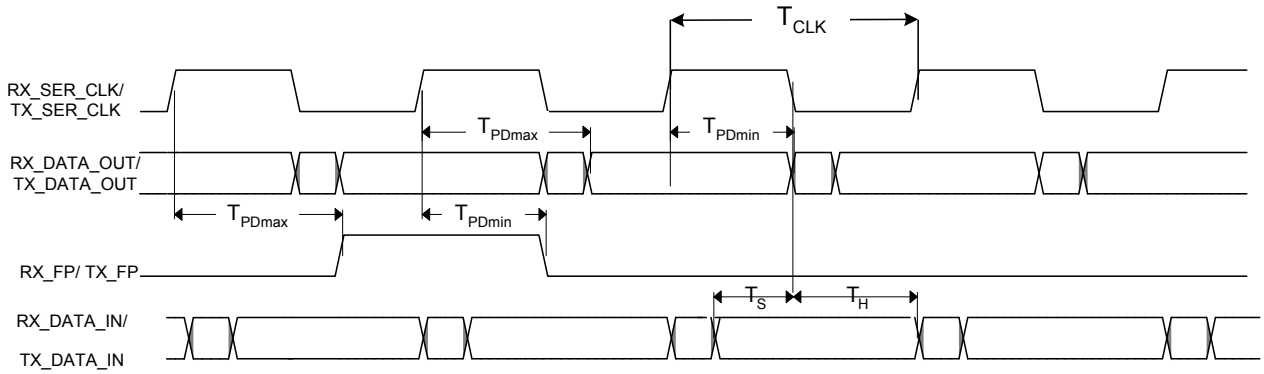


Figure 74: TOH Timing Diagrams

Table 34: TOH AC Characteristics

Parameter List	Symbol	Min	Max	Units
RX_SER_CLK & TX_SER_CLK period	T_{CLK}	193		ns
Receive				
RX_DATA_OUT/ RX_FP/ TX_DATA_OUT/ TX_FP propagation delay in respect to RX_SER_CLK /TX_SER_CLK	T_{PD}	93	97	ns
Transmit				
RX_DATA_IN/TX_DATA_IN Setup time in respect to RX_SER_CLK /TX_SER_CLK	T_S	10		ns
RX_DATA_IN/TX_DATA_IN Hold time in respect to RX_SER_CLK /TX_SER_CLK	T_H	10		ns

6.2.6 GPI

6.2.6.1 Asynchronous GPI with GPM (Internal Framer)

The following figure illustrates a payload source/sink connection via an asynchronous GPI, using the internal framer (GPM):

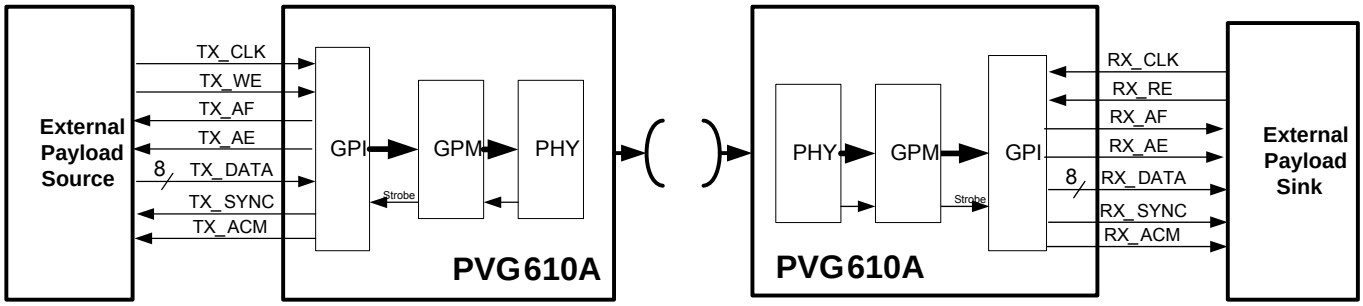


Figure 75: Asynchronous GPI with GPM

In using the internal framer (GPM), payload transferred through the GPI is muxed with other tributaries payloads on a single frame.

In asynchronous GPI modes, the air symbol clock is free running (locked on the DAC clock). The adaptation between the GPI traffic source/sink rate and the modem transfer rate is done by with FIFO's in the GPI RX/TX ports and flow control signals.

At the transmit side, TX_WE (TX Write Enable) signal is asserted whenever data is valid.

TX_AE (TX Almost Empty) and TX_AF (TX Almost Full) flags enable the external payload source to control the data flow, ensuring that the TX FIFO in the PVG610A is not under run or over run.

The TX_ACM line is used by the PVG610A to inform the external payload source of the ACM profile about to be used. As the TX_ACM signal indicates the setting of a new ACM profile, the external payload source has to adjust to the new ACM profile after one frame. The ACM profile is transferred to the payload source as a sequence of four bits (LSB first) starting 2 clock cycles after the TX_SYNC pulse. Note that TX_SYNC signal is not located in a fixed place with respect to the incoming data bytes.

At the receive side, the RX_RE (RX Read Enable) signal is asserted as the external payload sink request to read data (the data byte will be valid for sampling at the following clock cycle).

RX_AE (RX Almost Empty) and RX_AF (RX Almost Full) flags enable the payload sink to control the data flow, ensuring the FIFO is not under run or over run.

The RX_SYNC is used by the PVG610A to mark the start of a new air frame (i.e. the data byte transferred over the GPI bus at the time of the RX_SYNC pulse is the first payload-byte, coded in the first code-block of the airframe).

The RX_ACM line is used by the PVG610A to inform the payload sink that the ACM profile is being transmitted in the current frame. As the RX_ACM signal indicates that a new ACM profile is about be used, the external payload sink has to adjust to the new ACM profile at the current frame (i.e. adjust the read rate via the GPI to the new ACM profile). The ACM profile is transferred to the payload sink as a sequence of four bits (LSB first) arriving in parallel to the third to sixth data bytes of the frame. Note that the location of the ACM bits (and the data bytes) with respect to the RX_SYNC pulse is not fixed and depends on RX_RE signal. Also note that the behavior of RX_ACM signal is different from TX_ACM signal (TX_ACM bits start always two clock cycles after TX_SYNC)

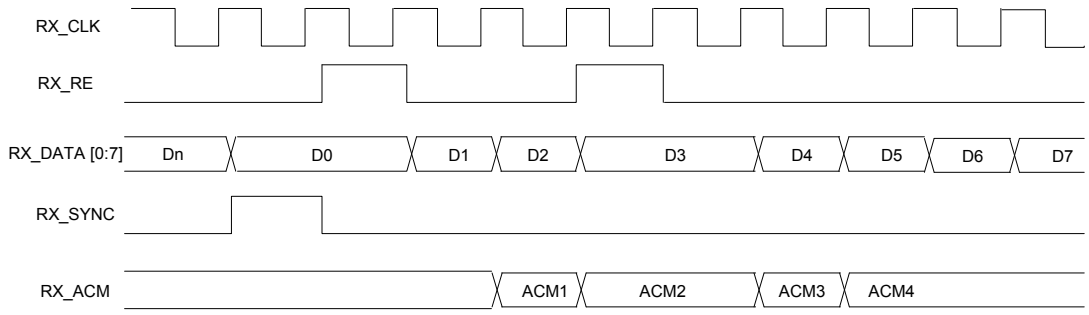


Figure 76: RX_ACM signal protocol

6.2.6.2 Asynchronous GPI with External Framer

The following figure illustrates the connection of an external framer via asynchronous GPI:

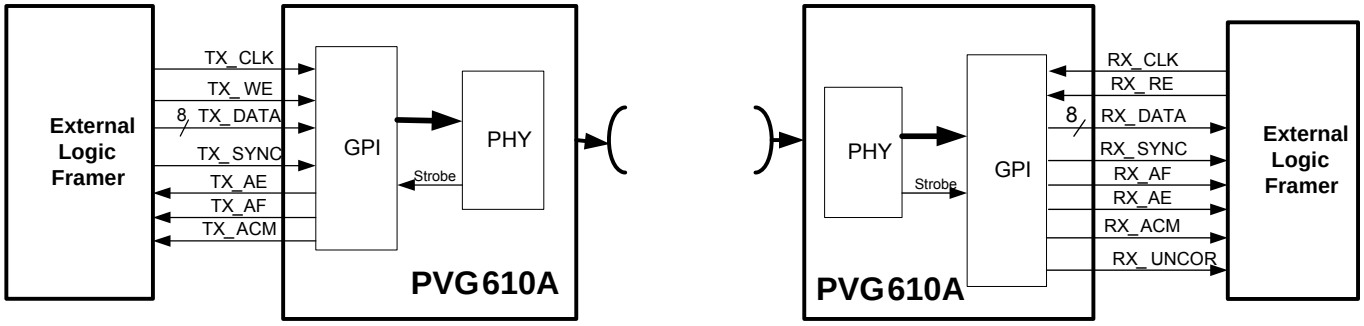


Figure 77: Asynchronous GPI with External Framer

When using an external framer the GPI is linked directly to the modem, bypassing the GPM

In asynchronous GPI modes, the air symbol clock is free running (locked on the DAC clock). The adaptation between the external framer payload rate and the modem transfer rate is aided with FIFO's in the GPI RX/TX ports and flow control signals.

The GPI protocol in this mode is similar to that of the Asynchronous GPI with GPM with the following differences:

- TX_SYNC is generated by the external framer and sent into the PVG610A (not from the PVG610A as the GPM case). TX_SYNC is used by the external framer to mark the start of new air frame (i.e. the data byte transferred over the GPI bus at the time of the TX_SYNC pulse is the first payload-byte coded in the first code-block in the airframe). The external framer has to coordinate its frame size with the configured PVG610A airframe size.
- The PVG610A aligns the ACM profile sequence to the incoming TX_SYNC (the sequence starts 3 clock cycles after the TX_SYNC pulse).
- RX_UNCOR signal is generated by the PVG610, accompanies all bytes that are part of LDPC or RS block, decoded with errors. This line is helpful when implementing external protection mechanism.
- ACM Pre notification can be programmed in the range of one to eight frames (instead of one frame always when using GPM)

6.2.6.3 Synchronous GPI with GPM (Internal Framer)

The following figure illustrates the payload connection source/sink via synchronous GPI, using the internal framer (GPM):

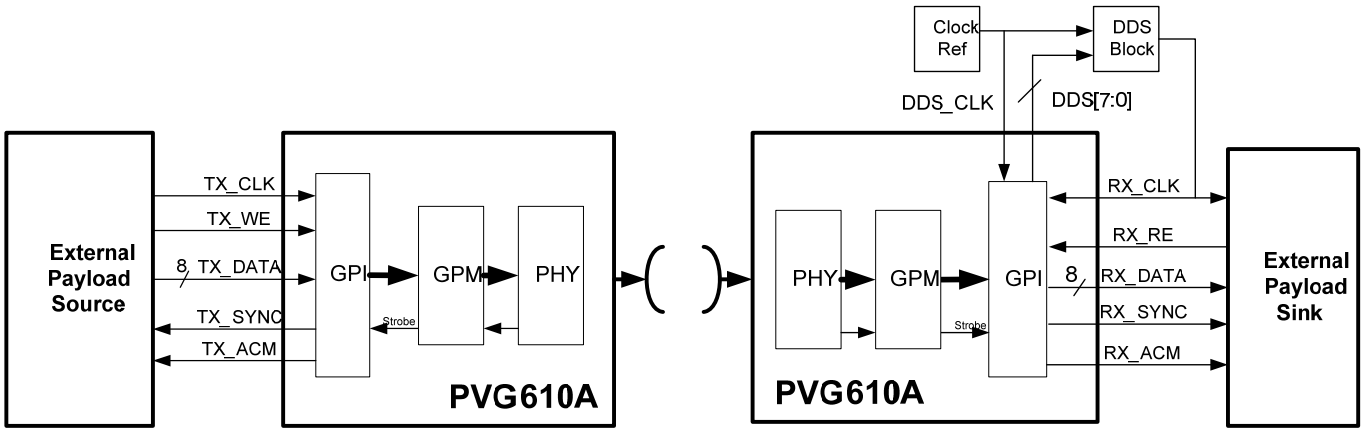


Figure 78: Synchronous GPI with GPM

When using the internal framer (GPM), payload from the GPI is muxed with other tributaries payloads on a single frame.

In synchronous GPI modes, data is transferred over the GPI at a constant rate (i.e. fixed number of bytes for a fixed number of TX/RX clock cycles).

In synchronous GPI at a GPM mode, the air symbol clock is locked on the DAC clock (as in asynchronous modes). In the TX side the adaptation between the GPI traffic source rate and the modem transfer rate is accomplished internally, in the PVG610, between the GPI and the GPM blocks (by means of stuffing bytes in the GPM frame). In the RX side, RX Clock is reconstructed with the external Direct Digital Synthesis (DDS) block (the clock frequency is set by an internal PLL locked on RX FIFO status). The PVG610A receives the DDS_CLK and supplies DDS [7:0] data to enable the clock construction. The PVG610A transfers samples from an internal sine wave look up table to the external DDS. The DDS clock rate has to be at least four times the desired synthesized clock frequency

AT the transmit side, TX_WE (TX Write Enable) signal is asserted as data is valid. When ACM is not used, or when using the highest ACM profile, TX_WE is set to ‘1’ (i.e. TX_CLK represents the actual byte rate). When ACM is used, TX_WE is a rational factor of TX_CLK. For example, to adjust a byte rate, which is 3 times slower than TX_CLK, TX_WE is set to ‘1’ for one TX_CLK clock period, every 3 TX_CLKs

The TX_ACM line is used by the PVG610A to inform the external payload source of the ACM profile about to be used. The external payload source then has to adjust to the new ACM profile after one frame. The ACM profile is transferred to the payload source as a sequence of four bits (LSB first) starting 2 clock cycles after the TX_SYNC pulse. Note that TX_SYNC signal is not aligned with the incoming data bytes.

At the receive side the RX_RE (RX Read Enable) signal is asserted as the external payload-sink requests to read data. When ACM is not used, or when using the highest ACM profile, RX_RE is set to ‘1’ (i.e. The RX_CLK represent the actual byte rate). When ACM is used, RX_RE is a rational factor of RX_CLK, for example, to adjust a byte rate, three times slower than RX_CLK, RX_RE is set to ‘1’ for one RX_CLK clock period every 3 RX_CLKs.

The RX_SYNC is used by the PVG610A to mark the start of a new air frame (i.e. the data byte transferred over the GPI bus at the time of the RX_SYNC pulse is the first payload-byte, coded in the first code-block of the airframe).

The RX_ACM line is used by the PVG610A to inform the external payload source of the ACM profile about to be used. When RX_ACM signal indicates that a new ACM profile is about to be used, the external payload sink has to be adjusted to that new ACM profile at the same frame, i.e. adjusting the read rate via the GPI to the new ACM profile. The ACM profile is transferred to the payload sink as a sequence of four bits (LSB first) arriving in parallel to the third to sixth data bytes of the frame (as described in details in 6.2.6.1 above.

6.2.6.4 Synchronous GPI with External Framer

The following figure illustrates the connection of an external framer to the PVG610A via synchronous GPI:

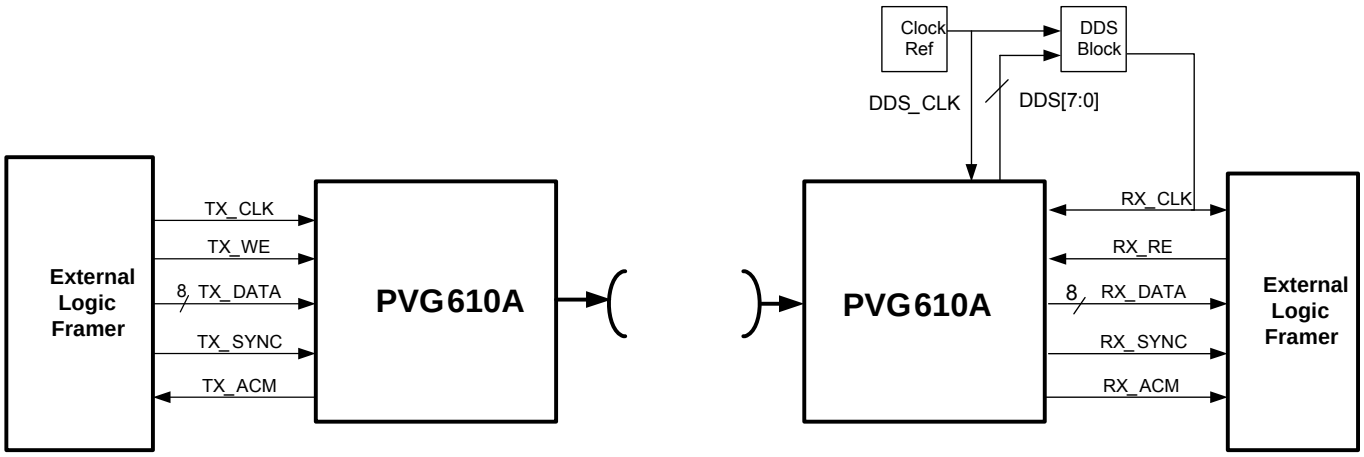


Figure 79: External Framer with Synchronous GPI

When using an external framer the GPI is linked directly to the modem, bypassing the GPM

In synchronous GPI modes, data is transferred through the GPI at a constant rate (i.e. fixed number of bytes for a fixed number of TX/RX clock cycles).

In a synchronous GPI with an external framer, the air symbol rate is locked on the TX_CLK signal (thus there is no need to adjust rates between the data source and the modem). At the receive side, similarly to the Synchronous GPI with GPM mode, the RX Clock is reconstructed with the external DDS. .

The GPI protocol in this mode is very similar to the previous case (Synchronous GPI with GPM). The differences are as follows:

- TX_SYNC is generated by the external framer sent to the PVG610A (not from the PVG610A as the GPM case). TX_SYNC is used by the external framer to mark the start of new air frame (i.e. the data byte transferred over the GPI bus at the time of the TX_SYNC pulse, is the first payload-byte in the first code-block in the airframe). The external framer has to coordinate its frame size with the configured PVG610A airframe size.
- The PVG610A aligns the ACM profile sequence with the incoming TX_SYNC (the sequence starts 3 clock cycles after the TX_SYNC pulse).
- RX_UNCOR signal is generated by the PVG610A and accompanies all bytes that are part of LDPC or RS blocks, decoded with errors. This line is helpful when implementing external protection mechanism.
- ACM Pre notification can be programmed in the range of one to eight frames (instead of one frame always when using GPM)

6.2.6.5 AC Characteristics

Note that the RX_UNCOR is a level signal which accompanies a group of bytes, decoded with errors, and not a pulse signal at the beginning of the frame as may be implied from the figure above.

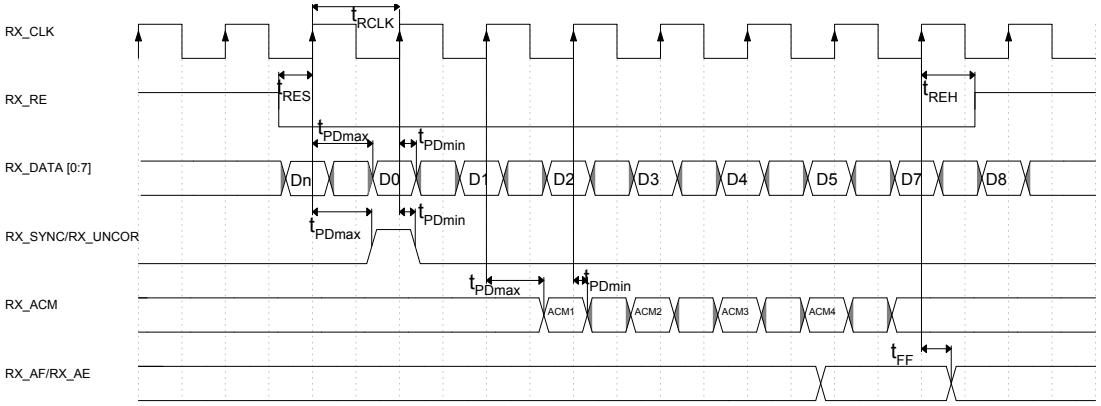


Figure 80: GPI Rx Timing Diagrams

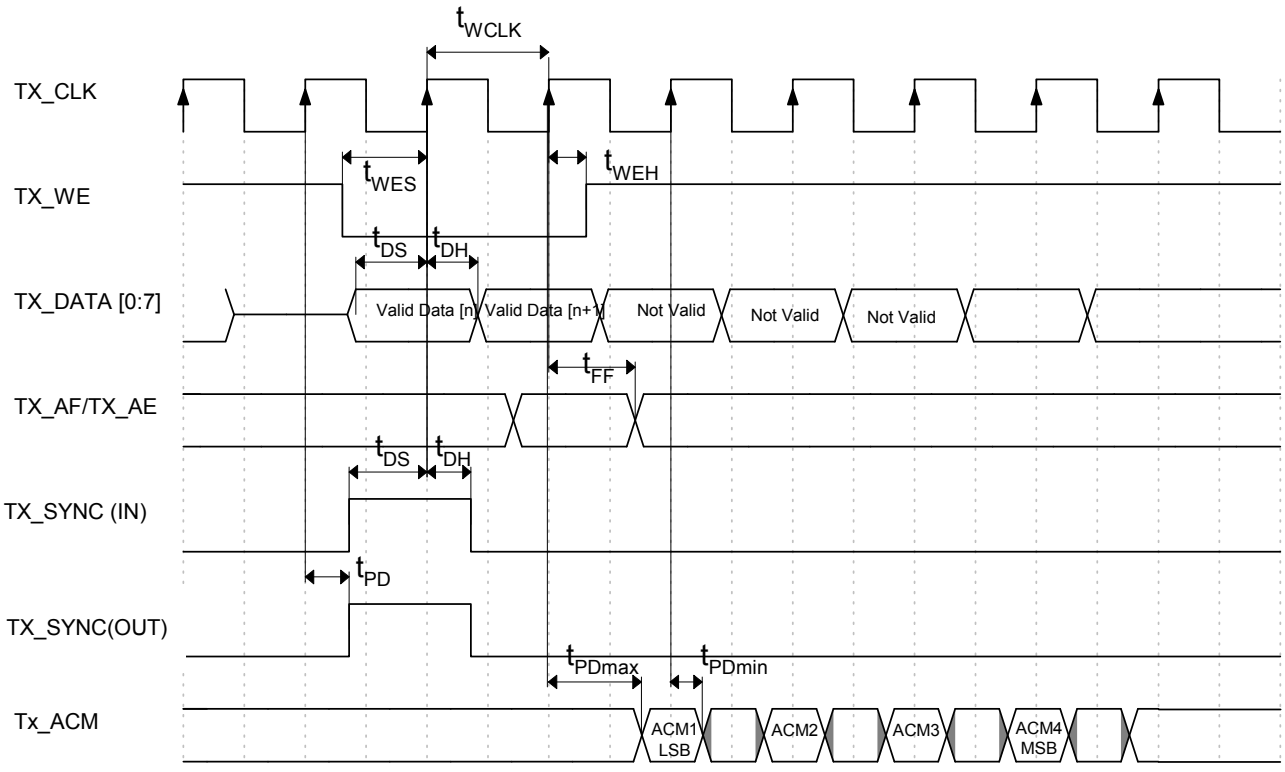


Figure 81: GPI Tx Timing Diagram

Note that when using the internal framer (GPM), the TX_SYNC output is not aligned with the data bytes (as may be implied from the diagram) and can be asserted at any point in time.

Table 35: GPI AC Characteristic

Parameter	Symbol	Min	Max	Units
Receive (RX) Interface				
Read clock period	t_{RCLK}	$4*t_{SYS}$		ns
RX_RE falling edge to RX_CLK rising edge setup time	t_{RES}	2		ns
RX_CLK rising edge to RX_RE rising edge hold time.	t_{REH}	0		ns
RX_CLK rising edge to RX_DATA [0:7], RX_SYNC/RX_UNCOR, RX_ACM propagation delay	t_{PD}	5	14	ns
RX_CLK rise to FIFO status flags	t_{FF}		8	ns
DDS_CLK Clock period	t_{DDS_CLK}	8.93		ns
DDS_CLK to DDS[0:7] propagation delay	t_{PD}	2.2	6.25	ns
Transmit (TX) Interface				
Write clock period	t_{WCLK}	$4*t_{SYS}$		ns
TX_WE falling edge to TX_CLK rising edge setup time	t_{WES}	1.5		ns
TX_CLK rising edge to TX_RE rising edge hold time.	t_{WEH}	1		ns
TX_DATA [0:7] , TX_SYNC (when input) to TX_CLK rising edge setup time	t_{DS}	1.5		ns
TX_CLK rising edge to TX_DATA [0:7], TX_SYNC (when input) hold time	t_{DH}	1		ns
TX_CLK rising edge to TX_ACM and TX_SYNC (when output) propagation delay	t_{PD}	5	12	ns
TX_CLK rise to FIFO flags	t_{FF}		8	ns

6.2.7 EOW Interface

The EOW interface supports the connection of external CODEC to the PVG610. The EOW interface can be mapped to:

- In-band EOW: Extraction/insertion of E1/E2 bytes of an STM-1 stream (optical side or air side)
- Out-of-band EOW: through the GPM frame

The following figure illustrates the CODEC connections with the PVG610.

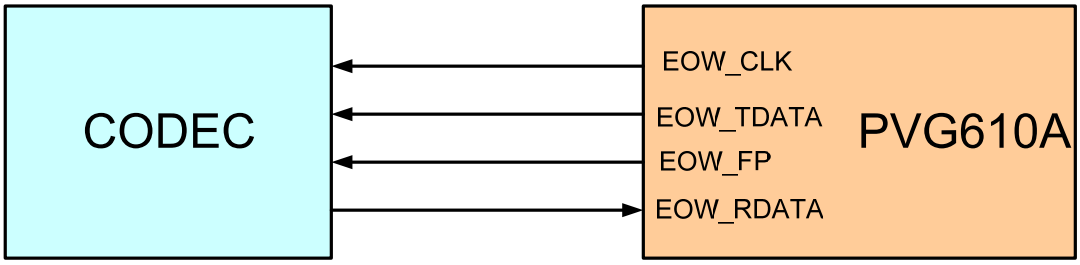


Figure 82: EOW CODEC connections with the PVG610

EOW_CLK is an integer division of the Sys_CLK, runs at 64Kbps or 128Kbps (when in inband, only 64kbps is supported).

The PVG610A samples data via the EOW_TDATA and EOW_RDATA lines every clock (the rising or falling edge can be used according to a predefined configuration). In the RX side bytes are discarded or duplicated to compensate for rate differences between the two sides of the radio.

EOW_FP (Frame Pulse) is an 8KHz signal representing the MSB bit of the data stream (both RX and TX). The frame pulse signal can be configured to be one or two EOW_CLK cycles long.

6.2.7.1 AC Characteristics

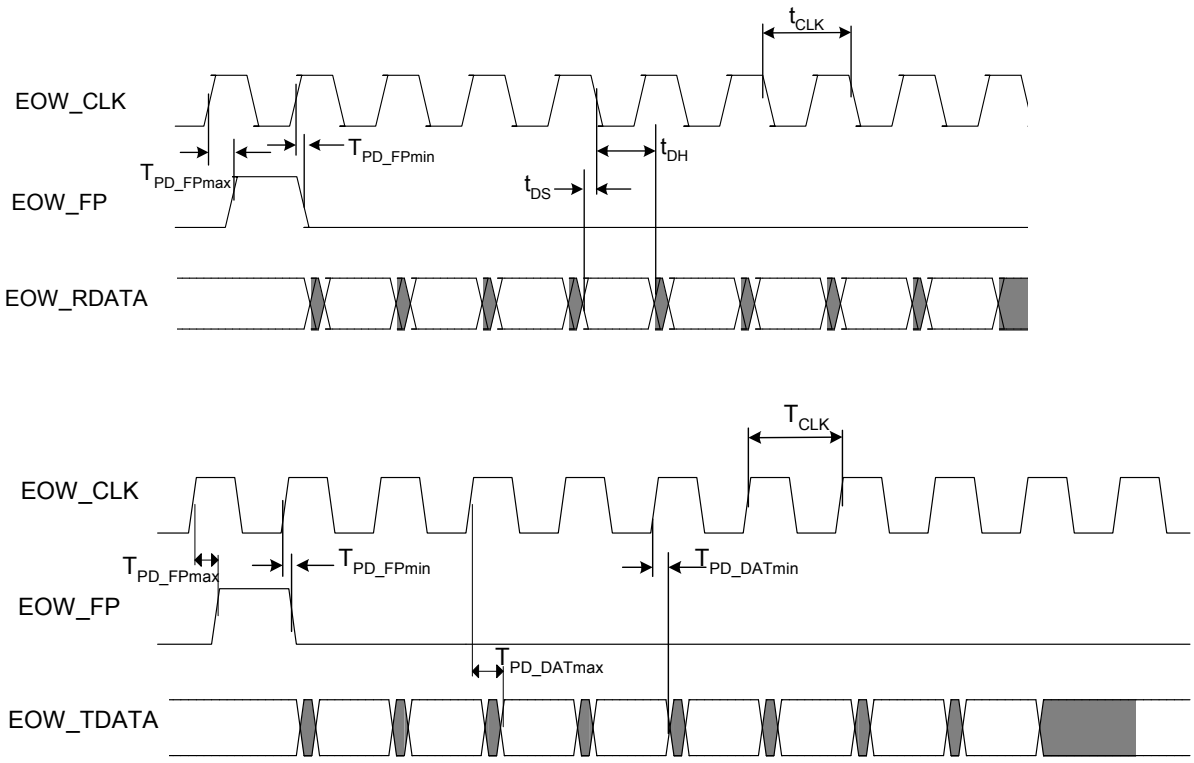


Figure 83: EOW Timing Diagrams

Table 36: EOW AC Characteristics

Parameter	Symbol	Min	Max	Units	Remarks
EOW_CLK period (output)		488	15,630	ns	
EOW_RDATA (input) to EOW_CLK falling edge Set up time	t_{DS}	45.5		ns	In respect to clock falling edge
EOW_CLK falling edge to EOW_RDATA (input) hold time	t_{DH}	29.5		ns	In respect to clock falling edge
EOW_CLK rising edge to EOW_TDATA (output) propagation delay	t_{PD_DAT}	495	500	ns	In respect to clock rising edge
EOW_CLK rising edge to EOW_FP (output) propagation delay	t_{PD_FP}	495	500	ns	In respect to clock rising edge

6.3 Management Interfaces

6.3.1 Host Interface

The Host interface is a parallel Data/Address interface. It is used by external device (e.g. external CPU) to communicate with the PVG610. It is also used by a PVG610X master to control a PVG610X slave.

The host interface supports two modes:

- Interleaved mode: the 16 data lines are used as address and data, alternatively. There are two cycles for each WRITE and READ operation. In the first cycle the address is asserted on the 16 data lines. In the second cycle the data is asserted on the data lines. The HOST_Address_0 line is used for alternating between address or data cycles. When HIGH the address is asserted, When LOW the data is asserted. When working with DPRAM, only one cycle of address is needed and then N x data cycles.
- Normal mode: the entire address and data fields, 16 bits each, are used and applied concurrently.

In both modes the control lines OE, WE and CS are active low.

Note that the interleaved mode is the default for the device. When booting via the Host Interface, the interleaved mode must be used for FW loading (see 5.3 above). After running the configuration file, the Host Interface mode can be changed to the Normal mode.

The two operating modes are illustrated in the following figures.

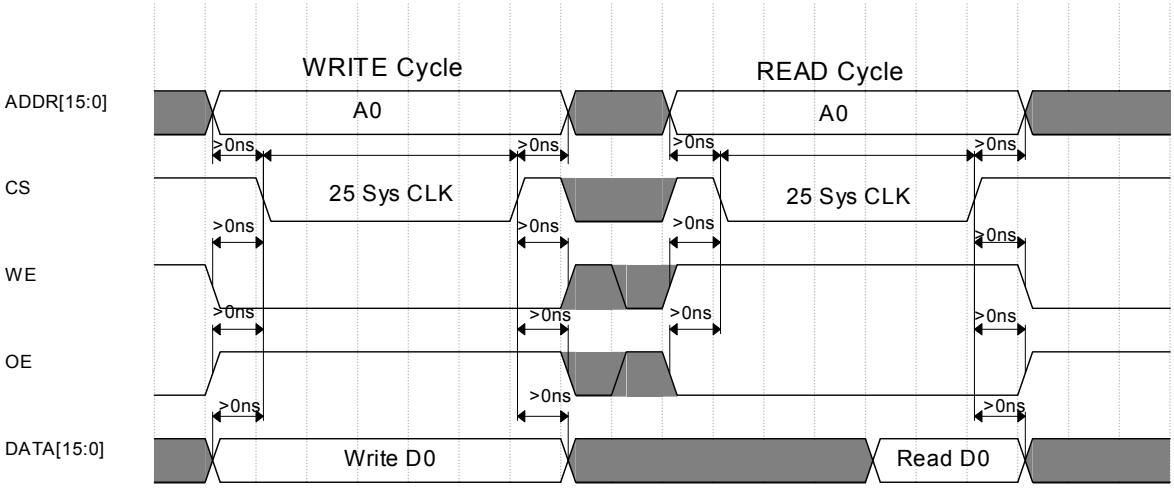


Figure 84: HOST Normal mode - Write and Read transactions

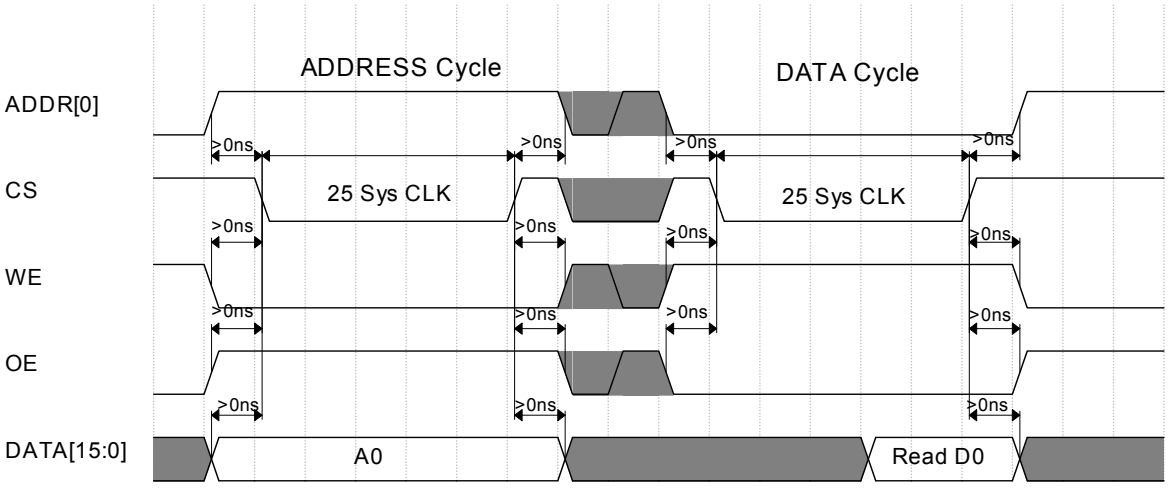


Figure 85: HOST Interleaved Mode Read transaction timing diagram,

The following figure illustrates the connection of an external CPU to the PVG610A via the host interface. The 15 MSB's of the address bus, colored gray, are optional (needed only in Normal mode)

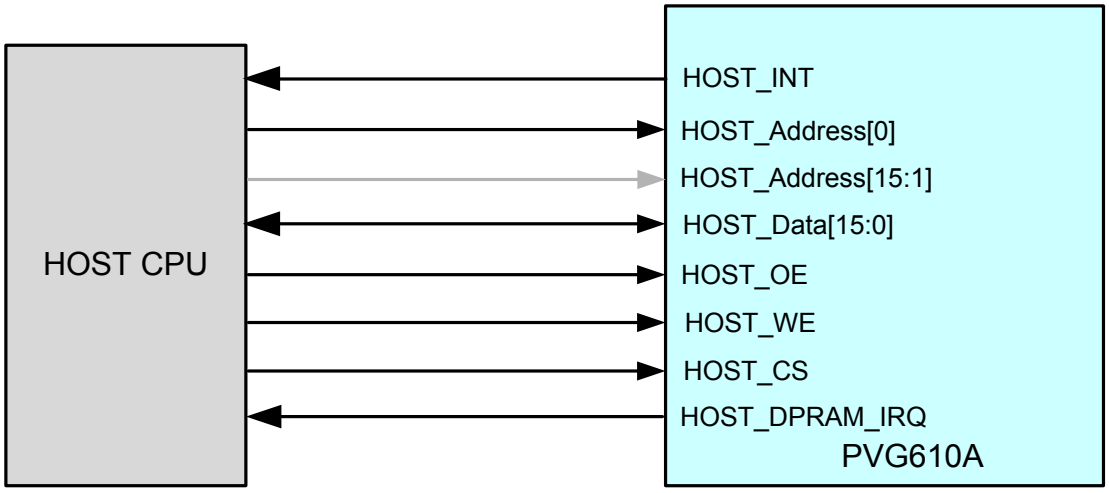


Figure 86: Connection of external CPU via Host Interface

In the XPIC architecture the HOST bus is used by the PVG610X Master to communicate with the PVG610A Slave. Hence the HOST CPU cannot be interfaced directly via the HOST bus. Two interface options are available for an external CPU;

1. Direct - the HOST CPU interface is conducted through the SPI or UART ports.
2. DPRAM – If a user wishes to maintain interfacing with the PVG610X via a HOST bus, an external DPRAM is added for isolation.

The following figure illustrates a management connection between two PVG610X devices in XPIC configuration while an external CPU is connected via the SPI or the UART interfaces. The 15 MSB's of the address bus, colored gray, are optional (needed only in Normal mode).

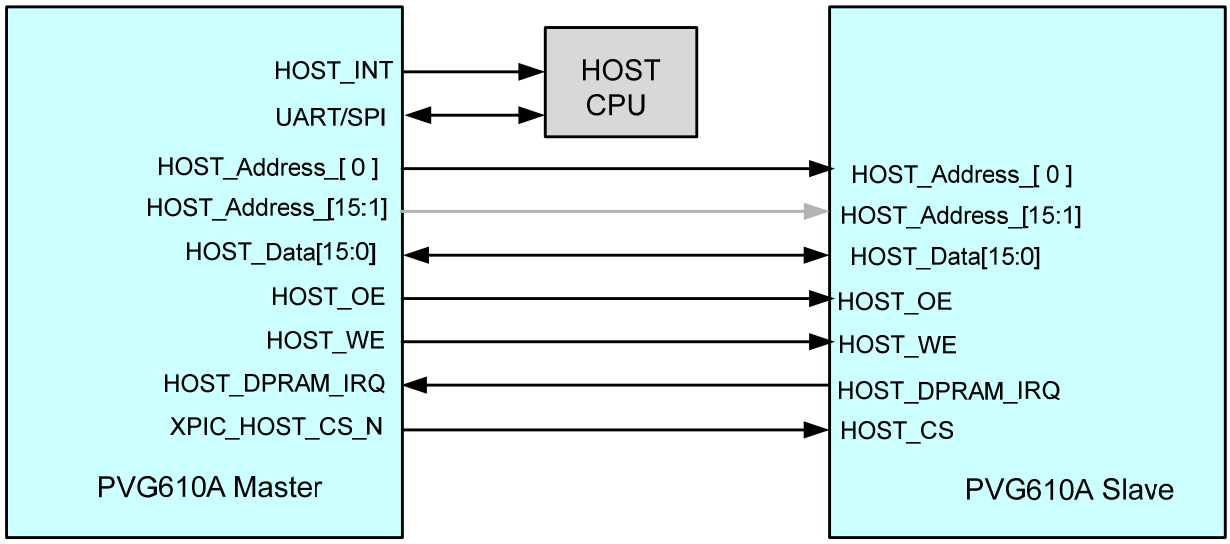


Figure 87: Host Interface in XPIC Configuration (Direct Mode)

The following figure illustrates a management connection between two PVG610X devices in XPIC configuration while an external CPU is connected via an external DPRAM. The 15 MSB's of the address bus, colored gray, are optional (needed only in Normal mode).

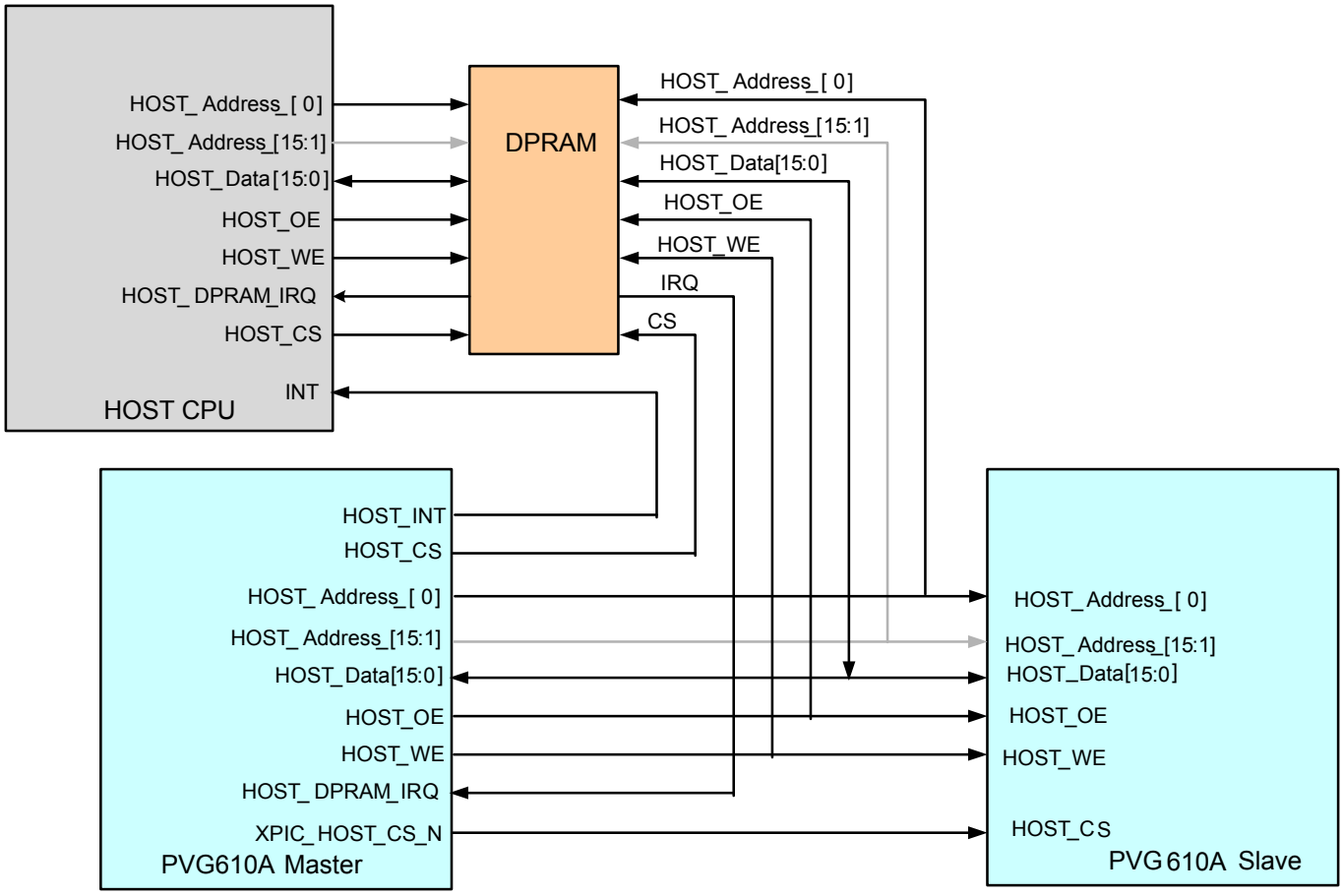


Figure 88: Host Interface in XPIC Configuration (DPRAM Mode)

6.3.1.1 AC Characteristics – Slave Mode

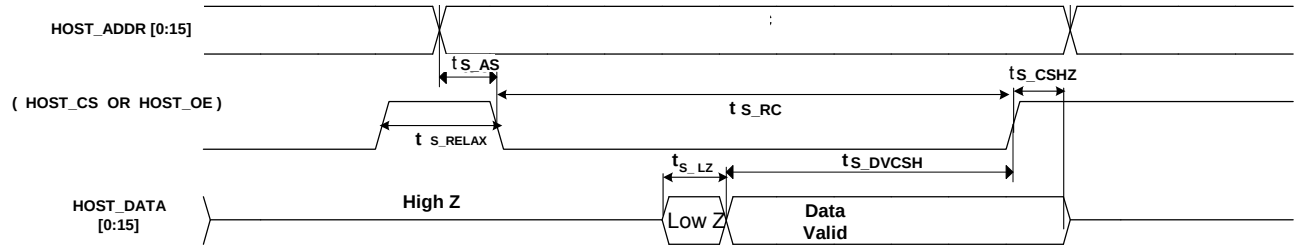


Figure 89: Slave Read cycle

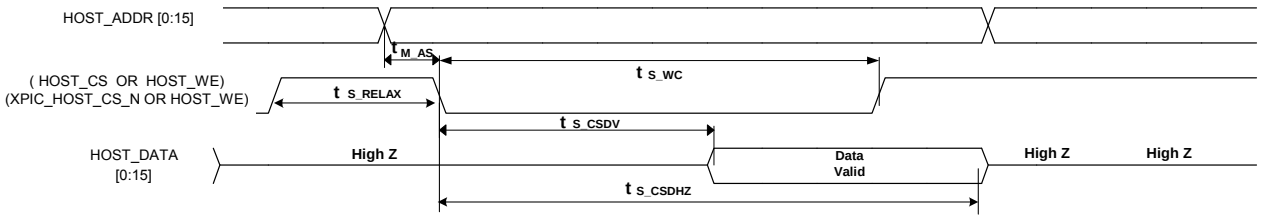


Figure 90: Slave Write

Table 37: Slave Host Timing Parameters

Parameter	Symbol	Min	Max	Units
Relax time between cycles	t_{S_RELAX}	30		ns
Read				
Read cycle	t_{S_RC}	25*t_{SYS}		ns
HOST_ADDR [0:15] to (HOST_CS OR HOST_OE) low setup time	t_{S_AS}		14.5*	ns
HOST_DATA [0:15] valid to(HOST_CS OR HOST_OE) high	t_{S_DVCSH}	18.5		ns
(HOST_CS OR HOST_OE) high to HOST_DATA [0:15] High Z	t_{S_CSHZ}	0.5		ns
HOST_DATA [0:15] in Low Z	t_{S_LZ}			ns
				ns
Write				
Write cycle	t_{S_WC}	25*t_{SYS}		ns
HOST_ADDR [0:15] to (HOST_CS OR HOST_OE) assertion setup time	t_{S_AS}		8.5	ns
(HOST_CS OR HOST_OE) assertion to HOST_DATA [0:15] valid	t_{S_CSDV}		19.5	ns
(HOST_CS OR HOST_OE) assertion to HOST_DATA [0:15] high Z	t_{S_CSDHZ}	23.5		ns

* It is required that the PVG610A will not need address setup greater then tAS

6.3.1.2 AC Characteristics – Master Mode

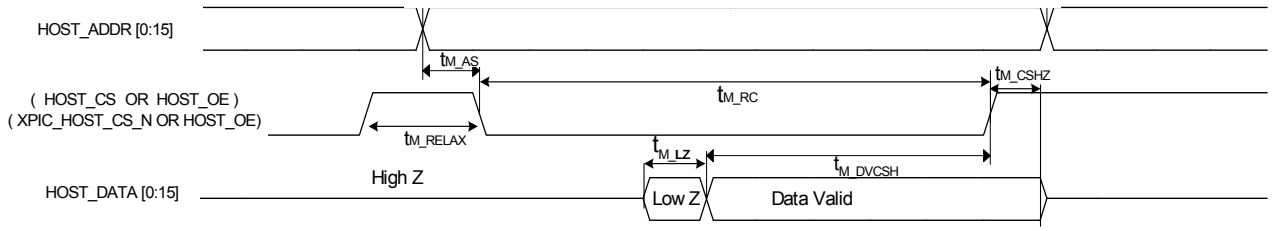


Figure 91: Master Read

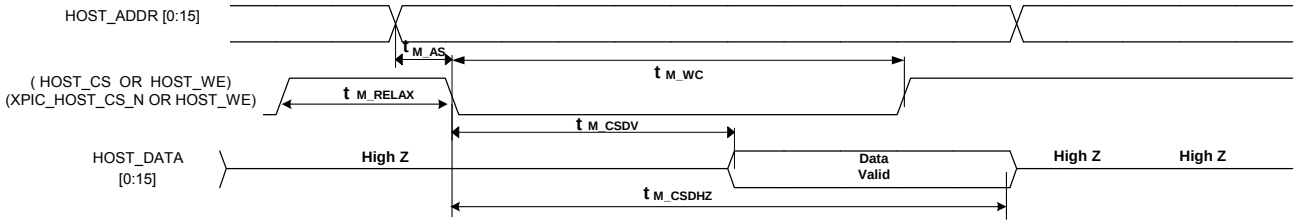


Figure 92: Master Write

Table 38: Host Timing Parameters (Master)

The PVG610A functions as a master when operating in an XPIC master mode.

Parameter	Symbol	Min	Max	Units
Relax time between cycles	t_{M_RELAX}			
Read				
Read cycle	t_{M_RC}	$25*t_{SYS}$		ns
HOST_ADDR [0:15] setup to (HOST_CS OR HOST_OE OR XPIC_HOST_CS_N) assertion	t_{M_AS}		14.5*	ns
HOST_DATA [0:15] valid to (HOST_CS OR HOST_OE OR XPIC_HOST_CS_N) high	t_{M_DVCSH}	18.5		ns
(HOST_CS OR HOST_OE OR XPIC_HOST_CS_N) High to HOST_DATA [0:15] high Z	t_{M_CSHZ}	0.5		ns
HOST_DATA [0:15] in Low Z	t_{S_LZ}			ns
Write				
Write cycle	t_{M_WC}	$25*t_{SYS}$		ns
HOST_ADDR [0:15] to (HOST_CS OR HOST_OE OR XPIC_HOST_CS_N) assertion setup time	t_{M_AS}		8.5	ns
(HOST_CS OR HOST_OE OR XPIC_HOST_CS_N) to HOST_DATA [0:15] valid	t_{M_CSDV}		19.5	ns
(HOST_CS OR HOST_OE OR XPIC_HOST_CS_N) to HOST_DATA [0:15] high Z	t_{M_CSDHZ}	23.5		ns

* Address setup must not exceed tAS

6.3.2 SPI

The Serial Peripheral Interface (SPI) bus is a 4-wire serial communications interface used by many microprocessor peripheral chips. The SPI is a synchronous serial data link used as a standard for connecting microprocessors and peripheral devices. The SPI bus is a master/slave type interface. As two devices communicate, one is referred to as the "master" and the other as the "slave". The master drives the serial clock. Data is concurrently transmitted and received, making SPI a full-duplex protocol.

The PVG610A has SPI-Master block (with 8 CS signals) and SPI-Slave block. The following figure illustrates the way in which the two blocks are connected to external pins.

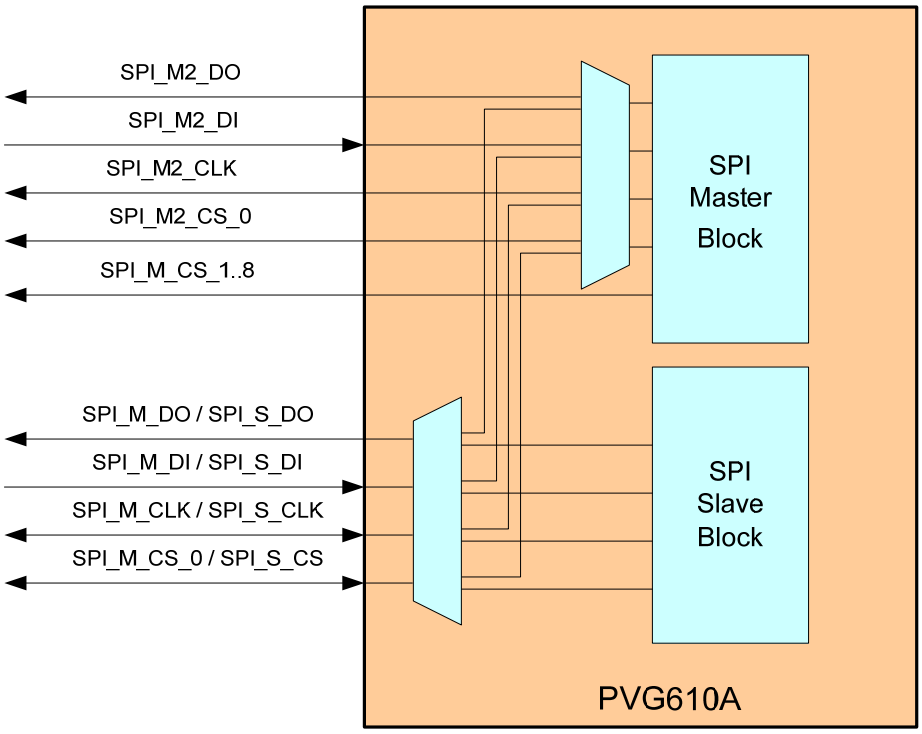


Figure 93: SPI Connections

Normally SPI_M2 signals are used as default for SPI master functionality (together with SPI_M_CS_1.to.8) and SPI_S signals are used for SPI slave functionality. SPI_M2 signals share the same pins with DC Correction signals. When DC Correction interface is used, the user can use the SPI_M for SPI master functionality.

The SPI slave interface of the PVG610A samples data in at the rising edge of the clock and samples data out at the falling edge of the clock. Between transactions the clock should remain at high level.

When booting from flash the SPI master interface of the PVG610A samples data in at the rising edge of the clock and samples data out at the falling edge of the clock. Between transactions the clock signal remains at high level.

When communicating with peripheral devices after boot process ends, the user can configure the SPI master interface, per transaction. The user controls the clock phase (sample at rising or falling edge of the clock) and the clock polarity between transactions.

6.3.2.1 SPI Master AC Characteristics

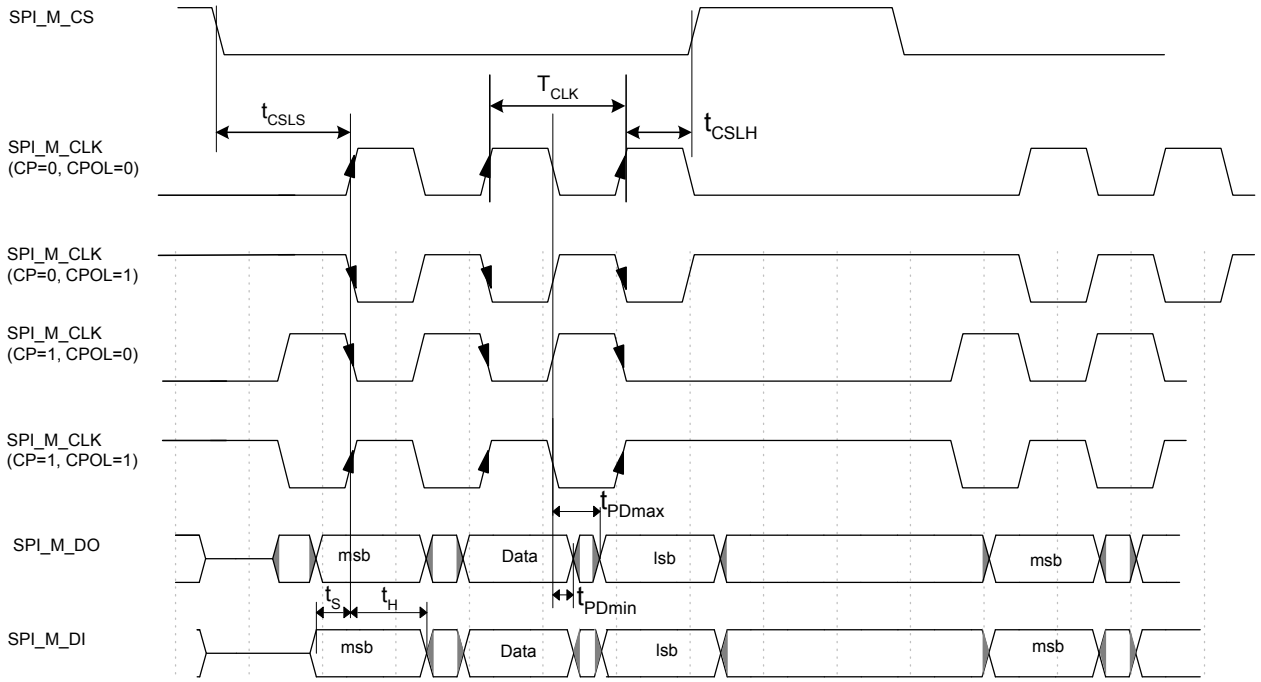


Figure 94: SPI Master Timing Diagram

Table 39: SPI Master AC Characteristics

Parameter	Symbol	Min	Max	Units	Remarks
Input					
SPI_M_DI to SPI_M_CLK setup time	t_S	25		ns	
SPI_M_CLK to SPI_M_DI hold time	t_H	5		ns	
Output					
SPI_M_CLK cycle period	T_{CLK}	Max{50ns, 2/Sys_Clk}		ns	
SPI_M_CLK edge to SPI_M_DO propagation delay	t_{PD}	20	25	ns	
SPI_M_CS_X low to SPI_M_CLK edge	t_{CSLS}	25		ns	
SPI_M_CLK edge to SPI_M_CS_X high	t_{CSLH}	5		ns	

6.3.2.2 SPI slave AC Characteristics

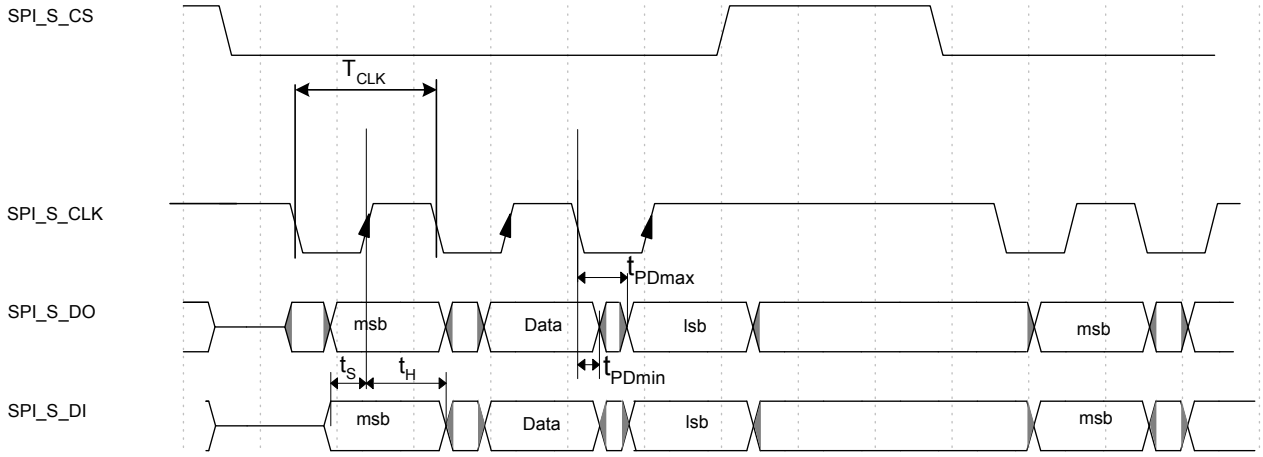


Figure 95: SPI Slave Timing Diagram

Table 40: SPI Slave AC Characteristics

Parameter	Symbol	Min	Max	Units	Remarks
Input					
SPI_S_CLK cycle period	T_{CLK}	Max{110ns, 8/Sys Clk}		ns	
SPI_S_DI to SPI_S_CLK setup time	t_S	25		ns	
SPI_S_CLK to SPI_S_DI hold time	t_H	5		ns	
Output					
SPI_S_CLK falling edge to SPI_S_DO propagation delay	t_{PD}	41	52	ns	
SPI_S_CS low to SPI_S_CLK setup time	t_{CSLS}	25		ns	

6.3.3 I2C

Inter Integrated Circuit (I2C) bus consists of 2 active wires and a ground connection. The active wires, SDA and SCL, are both bi-directional. SDA is the Serial Data line and SCL is the Serial Clock line.

With I²C, each IC on the bus has a unique address. Devices can act as a receiver and/or transmitter depending on its functionality.

A device that controls signal transfers on the line in addition to controlling the clock frequency is the master whereas a device controlled by the master is the slave. The master can transmit or receive signals to or from a slave, respectively, or control signal transfers between two slaves, where one is the transmitter and the other is the receiver. The I2C bus supports more than one master connected to one bus.

The I2C bus provides the flexibility to create a multi-master environment. It is possible to combine several masters, in addition to several slaves, onto an I²C-bus to form a multi-master system. If multiple masters simultaneously attempt to control the line, an arbitration procedure is used to determine priorities.

To begin communication, the bus master (typically a microcontroller) places the address of the device with which it intends to communicate (the slave) on the bus. All ICs monitor the bus for their address. Only the addressed device communicates with the master.

- The PVG610A has an I2C block supporting the following features:
- Two speeds:
- Standard mode (100 Kb/s)
- Fast mode (400 Kb/s)
- Master or slave I2C operation.
- 7- or 10-bit addressing.
- Ignores CBUS addresses (an older ancestor of I2C that used to share the I2C bus).

The I2C by definition is a 5 V based, nevertheless, the PVG610A drives the I2C with a 3.3V.

6.3.3.1 AC Characteristics

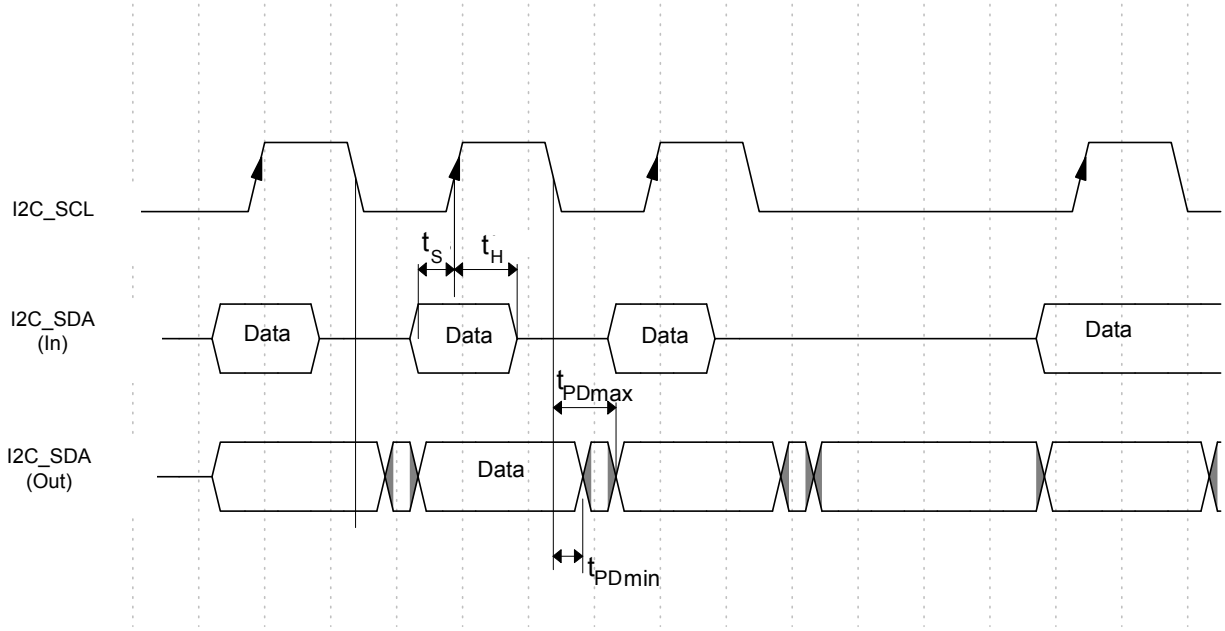


Figure 96: I2C BUS Timing

Table 41: I2C AC Characteristics Standard Mode:

Parameter	Symbol	Min	Max	Units	Remarks
Transmit					
Data changing to clock starts to rise	t_{1min}	1250		ns	
Clock starts to fall to data changing	t_{2min}	3750		ns	
Clock starts to rise to data starts to fall	t_{3min}	5700		ns	for Repeated Start
Data starts to fall to clock starts to fall	t_{4min}	4300		ns	for Repeated Start
Clock starts to rise to data starts to rise	t_{5min}	5000		ns	for Stop
Clock finishes to fall and data changing	t_6	0	3450	ns	
I2C_SCL falling edge to I2C_SDA propagation delay	t_{PD}	40	50	ns	
Receive					
Data hold time	t_S	10		ns	
Data setup time	t_H	50		ns	

Table 42: I2C AC Characteristics Fast Mode:

Parameter	Symbol	Min	Max	Units	Remarks
Transmit					
Data changing to clock starts to rise	t_{1min}	400		ns	
Clock starts to fall to data changing	t_{2min}	1200		ns	
Clock starts to rise to data starts to fall	t_{3min}	900		ns	for Repeated Start
Data starts to fall to clock starts to fall	t_{4min}	900		ns	for Repeated Start
Clock starts to rise to data starts to rise	t_{5min}	900		ns	for Stop
Clock finishes to fall and data changing	t_6	0	900	ns	
I2C_SCL falling edge to I2C_SDA propagation delay	t_{PD}	40	50	ns	
Receive					
Data hold time	t_S	10		ns	
Data setup time	t_H	50		ns	

6.3.4 UART

The PVG610A has a UART interface for management, using Hipper Terminal common method application, such as RS-232/422. The UART interface supports the following features:

- Full duplex operation
- Baud rate: 115KBPS
- Configurable character size definition - 5, 6, 7 and 8 bits per character.
- Configurable Parity – odd, even and no parity.
- Configurable number of stop bits – 1 or 2.

Note: PVG610A provides only RX and TX data as pin-out signals (with LVCMOS I/O's).

6.3.5 OMI

The Out-band Management Interface allows two CPU's across the radio link to communicate via a dedicated channel muxed within the GPM frames (The OMI is not available in GPM bypass mode).

The interface consists of four lines:

- OMI_TXD – Transmit data (input to the PVG610)
- OMI_TCLK – Transmit clock signal (output from the PVG610)
- OMI_RCLK - Receive clock signal (output from the PVG610)
- OMI_RXD – Receive data (output from the PVG610)

The OMI nominal clock period is built out of N x system clock periods (N >= 8). TCLK period is constant and equal to the OMI nominal clock period. RCLK period is changed in time to accommodate the incoming OMI traffic from the radio side. The RCLK period can be equaled to the OMI nominal period or, one system clock period more than that or one system clock period less than that.

The max clock rate (SysClock/(N-1)). is below 10MHz

The OMI interface can be configured to work on the rising edge or falling edge.

6.3.5.1 AC Characteristics

The figure below describes the timing diagram when the OMI is configured to work with rising edge of clocks. When falling edge is selected, the clock in the diagram should be inverted.

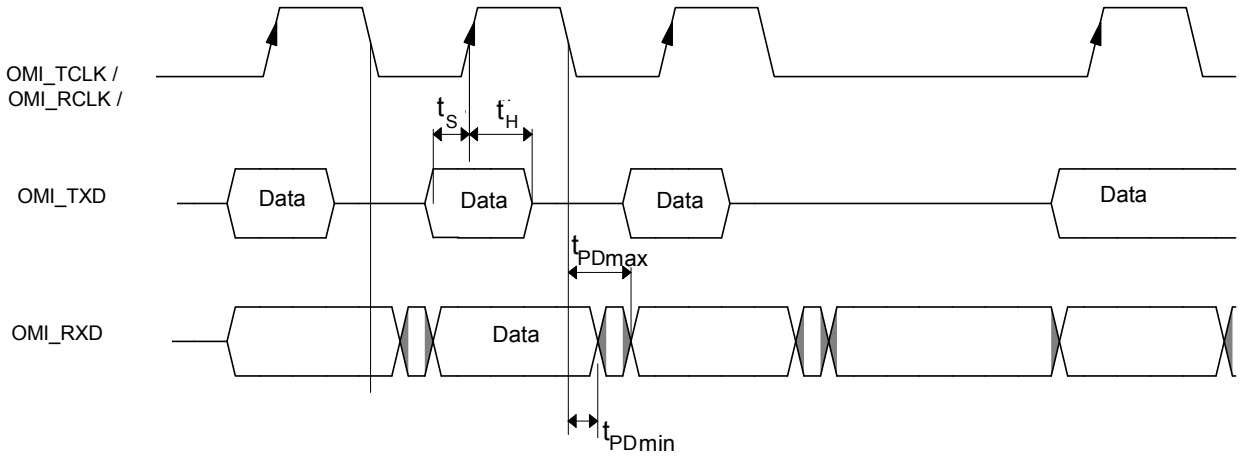


Figure 97: OMI Timing Diagrams

Table 43: OMI AC Characteristics

Parameter List	Symbol	Min	Max	Units
OMI_TCLK & OMI_RCLK period	t_{CLK}	100		ns
Receive				
OMI_RXD Output data propagation delay in respect to OMI_RCLK rising/falling edge	t_{PD}	50	60	ns
Transmit				
OMI_TXD Input data set up time* in respect to OMI_TCLK rising/falling edge	t_S	10		ns
OMI_TXD Input data hold time in respect to OMI_TCLK rising/falling edge	t_H	10		ns

6.3.6 HDLC

HDLC is used to open a management communication link between the two PVG610A CPU's (at the two sides of the radio link) when using GPI with external framer (bypassing the GPM). The objective is to create a link between the internal CPU in the local PVG610A station with the internal CPU at the remote PVG610A station. The HDLC frame byte is muxed with the external framer frames entering the GPI interface.

The HDLC signals are:

- HDLC_TXD - Transmit data (output from the PVG610)
- HDLC _TCLK - Transmit clock signal (input to PVG610)
- HDLC _RCLK - Receive clock signal (input to PVG610)
- HDLC _RXD - Receive data (input to PVG610)

The max clock rate has to be below 10MHz (max clock rate is SysClock / M , where M >=10). The HDLC interface complies with ISO 13239.

6.3.6.1 AC Characteristics

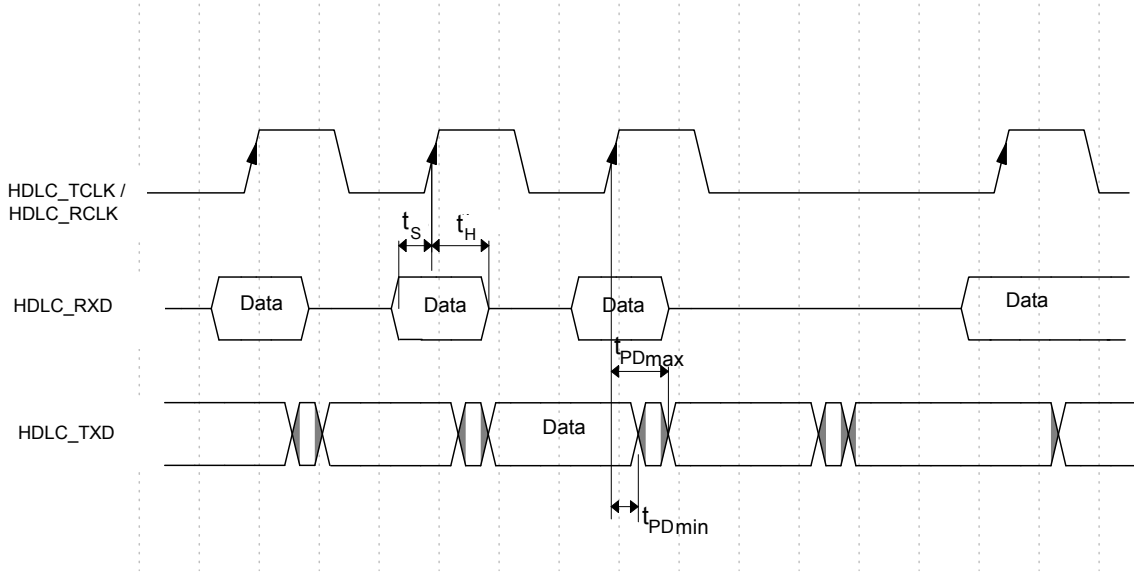


Figure 98: HDLC Timing Diagrams

Table 44: HDLC AC Characteristics

Parameter List	Symbol	Min	Max	Units
HDLC_TCLK & HDLC_RCLK period	t_{CLK}	100		ns
Transmit				
Output data HDLC_TXD propagation delay in respect to HDLC_TCLK	t_{PD}	9.84	23.9	ns
Receive				
Input data HDLC_RXD set up time in respect to HDLC_RCLK	t_S	2		ns
Input data HDLC_RXD hold time HDLC_RCLK	t_H	0		ns

6.4 AFE Interface

6.4.1 Baseband/IF Dual 12-bit ADC

The dual ADC is comprised of two identical 12 bit ADC blocks operating in one of the following modes:

- Base Band: two analog inputs (I and Q) are sampled concurrently. The maximum sampling frequency is 100MHz.
- IF: One of the two ADC devices can be used for IF sampling at a maximum rate of up to 200MHz. These ADC devices are optimized to work at rates of up to 160MHz. Conversion at 200MHz rate is supported but with reduced performance compared to that of the 160MHz.

The following pins are used with the dual ADC:

ADC_CLK_N/P – ADC	clock input. LVPECL levels
BB_IN_I_N/P BB_IN_Q_N/P	differential analog input signals
VCM_I, VCM_Q	common mode voltage output
ADC_CLK_VDD1P2 ADC_CLK_VSS	1.2 V voltage supply and ground for the clock network
ADC_VDD1P2	1.2 V voltage supply for the ADC core
ADC_VDD3P3	3.3 V voltage supply for the ADC input stage
ADC_VSS	ground for the core and input stage supplies

The ADC_VDD1P2 supply pin, to be connected to 100 nF capacitor in parallel with 1 nF capacitor.
The ADC_CLK_VDD1P2 supply pin, to be connected to 100 nF capacitor in parallel with 1 nF capacitor.

The ADC power consumption is roughly proportional to the conversion rate, so at half the conversion rate the power dissipation is also reduced by about a half.

The aperture jitter on the clock is a critical parameter for ADCs sampling of high frequencies input signal. The aperture jitter on the clock is a wide band noise. This noise is sampled and folded into the output spectrum. The SNDR of the ADC is degraded with this noise.

For low performance applications a single ended clock may be used instead of the differential input clock. The single ended ADC clock name is SPARE0 .

The ADC block has a division by two option (i.e. the ADC_CLK signal is divided by two before it enters the ADC block). This, in some cases, enables the use a single clock source for both DAC and ADC without an external divider.

DC or AC coupling can be used in the ADC input. An example of a DC coupled input configuration using an off-chip amplifier is shown in the following figure. An RC network at the input is used to reduce the output bandwidth of the source amplifier and dampen oscillations that may occur due to inductances on the PCB and the package. The output common mode of the driving amplifier should be controlled by VCM output. A termination resistor (RT) may be used if necessary.

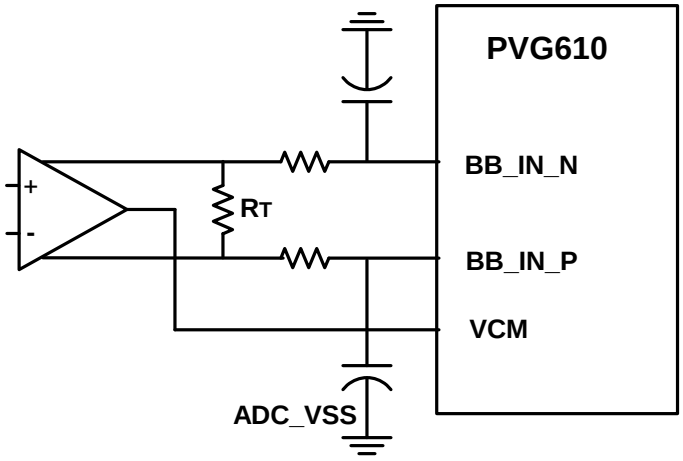


Figure 99: ADC Differential DC Coupled Connection

For an IF configuration an AC coupling connection may be used. An AC coupled input can be implemented using a transformer with a center tapped secondary winding. As shown below, the center tap is connected to the common mode output pin. An RC low pass network may be used to reduce oscillations. Termination resistors may be used if necessary.

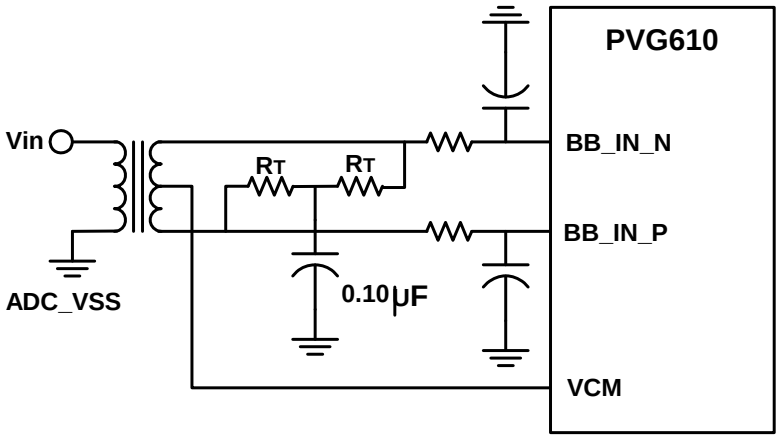


Figure 100: ADC Differential AC Coupled Connection

6.4.1.1 DC Specifications

(At TA = 25 ºC, VAVDD1V2 = 1.2V, VAVDD3V3 = 3.3V, FCLK = 160 MSPS, FIN = 14 MHz, 1.0 V p-p differential full-scale input signal, data per channel unless otherwise specified)

Table 45: Baseband IF ADC DC Specification

Parameter (condition)	Min	Typ	Max	Units
DC Accuracy				
Resolution	12			Bits
No Missing Codes Guaranteed	12			Bits
Integral Non Linearity [1]		± 1		LSB
Differential Non Linearity [2]		± 0.5		LSB
Gain Error (±3σ) [3]			9	% FSR
Gain Matching (±3σ) [4]			3	% FSR
Offset Error [5]			10	mV
Analog Input				
Input Differential Voltage Range	± 475	± 500	± 540	mV
VCM output voltage	0.9	1.1	1.3	V
Max Allowed VCM Current	10			ua
Input Common Mode Voltage	VCM-50mV	VCM	VCM+50mV	
Input Impedance, differential		60		k ohm
Analog Input Bandwidth	700	1000		MHz

1. The deviation of the ADC transfer function from the ideal transfer function.
2. In an ideal ADC every code transition to its neighbors equals to 1 LSB. DNL is the deviation of each code transition from the ideal value.
3. The deviation of the actual difference between the first and last code transition and the ideal difference.
4. Gain difference between the two channels.
5. Mid code ideally occurs for zero differential input. The offset error is the differential input voltage that results in mid code.

6.4.1.2 Dynamic Specifications

(At TA = 25 ºC, VAVDD1V2 = 1.2V, VAVDD3V3 = 3.3V, FCLK = 160 MSPS, FIN = 14 MHz, , 1.0Vp-p differential full-scale input signal, data per channel unless otherwise specified)

Table 46: Baseband IF ADC Dynamic Specification

Parameter (condition)	Min	Typ	Max	Units
SWITCHING PERFORMANCE				
Conversion Rate	16		200	MSPS
Input Clock Duty Cycle	15		85	%
Aperture Uncertainty (Jitter)		0.8		ps rms
Out-of-Range Recovery Time [1]		2		clocks
SIGNAL-TO-NOISE-AND-DISTORTION RATIO [2]				
100 MSPS, FIN = 9.95MHz		57		dBFS
160 MSPS, FIN = 9.95MHz		58.5		dBFS
160 MSPS, FIN = 200 MHz		50.1		dBFS
SPURIOUS FREE DYNAMIC RANGE [3]				
100 MSPS, FIN = 9.95 MHz		71		dBc
160 MSPS, FIN = 9.95 MHz		72		dBc
160 MSPS, FIN = 200 MHz		56.5		dBc
EFFECTIVE NUMBER OF BITS				
100 MSPS, FIN = 9.95 MHz		9.2		Bit
160 MSPS, FIN = 9.95 MHz		9.4		Bit
160 MSPS, FIN = 195 MHz		8.2		Bit
TWO TONE INTERMODULATION [4]				
160 MSPS, FIN1,2 = 9.5, 10.5 MHz		75		dBc
160 MSPS, FIN1,2 = 19, 20 MHz		75		dBc
CHANNEL ISOLATION [5]				
160 MSPS, FIN = 100 MHz		60		dBc

1. The time required for the ADC to return to specified characteristics after an out-of-range sample.
2. The SNDR is the rms ratio of the measured input signal to the sum of all other spectral harmonics excluding the dc component
3. The SFDR is the amplitude difference between the measured input signal and the highest harmonic component.
4. The IMD is the rms ratio between the sum of the input signals and the highest harmonic component.
5. Coupling into one channel with a –40 dBFS input signal from the other channel driven by a full-scale input signal.

6.4.2 IF Sampling 10-bit ADC

Direct IF: The PVG610A has additional ADC supporting direct IF mode. The input clock is up to 200 MHz.

The following pins are used with the IF ADC:

ADC_CLK_N/P	ADC clock input. LVPECL levels
IF_IN_N/P	Differential analog input signal
ADC_CLK_VDD1P2, ADC_CLK_VSS	1.2 V voltage supply and ground for the clock network
ADC_VDD1P2	1.2 V voltage supply for the ADC core
ADC_VDD3P3	3.3 V voltage supply for the ADC input stage
ADC_VSS	ground pin for the core and input stage supplies

The ADC_VDD1P2 supply pin is to be connected to 100 nF capacitor in parallel with 1 nF capacitor.

The aperture jitter on the clock is a critical parameter for ADCs sampling of high input signal frequencies. Aperture jitter on the clock is a wide band noise. This noise is sampled and folded into the output spectrum. The SNDR of the ADC is degraded with this noise.

For low performance applications a single ended clock may be used instead of the differential input clock. The single ended ADC clock name is SPARE0.

The ADC block has a division by two option (i.e. ADC_CLK signal is divided by two before it enters the ADC block).

Unused IF input pins should be left unconnected.

The IF ADC should be connected using AC coupling. An AC coupled input can also be implemented using a transformer with a center tapped secondary winding. As shown below, the center tap is connected to the common mode output pin. An RC low pass network may be used to reduce oscillations. Termination resistor may be used if necessary.

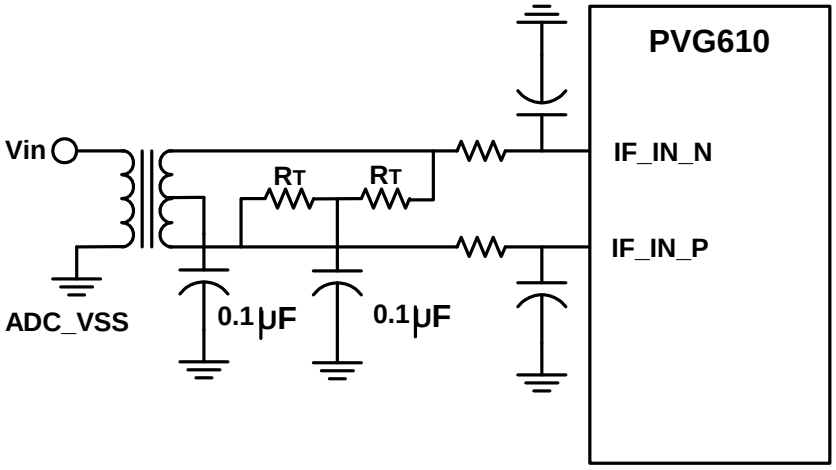


Figure 101: ADC Differential AC Coupled Connection

6.4.2.1 DC Specifications

(At TA = 25 ºC, VAVDD1V2 = VVDD = 1.2 V, VAVDD3V3 = 3.3 V, FCLK = 205 MHz, FIN = 10 MHz, 1.0 V p-p differential full-scale input signal unless otherwise specified)

Table 47: IF Sampling ADC DC Specifications

Parameter (condition)	Min	Typ	Max	Units
DC ACCURACY				
Resolution	10			Bits
No Missing Codes Guaranteed	10			Bits
Integral Non Linearity [1]		± 1		LSB
Differential Non Linearity [2]		± 0.6		LSB
Gain Error (±3σ) [3]			7	% FSR
Offset Error [4]		TBD		mV
ANALOG INPUT				
Input Differential Voltage Range	± 0.25		± 0.5	V
Input Capacitance			0.03	pF
Input Resistance		20		kOhm
Analog Input Bandwidth	400			MHz
AC coupling lower cutoff frequency			500	kHz

1. The deviation of the ADC transfer function from the ideal transfer function.
2. In an ideal ADC every code transition to its neighbors equals to 1 LSB. DNL is the deviation of each code transition from the ideal value.
3. The deviation of the actual difference between the first and last code transition and the ideal difference.
4. Mid code ideally occurs for zero differential input. The offset error is the differential input voltage that gives mid code.

6.4.2.2 Dynamic Specifications

(At TA = 25 ºC, VAVDD1V2 = VVDD = 1.2 V, VAVDD3V3 = 3.3 V, FCLK = 205 MHz, FIN = 10 MHz, , 1.0Vp-p differential full-scale input signal unless otherwise specified)

Table 48: IF Sampling ADC Dynamic Specifications

Parameter (condition)	Min	Typ	Max	Units
SWITCHING PERFORMANCE				
Maximum Conversion Rate	205			MSPS
Minimum Conversion Rate			30	MSPS
Input Clock Duty Cycle	15	50	85	%
Aperture Uncertainty (Jitter)		1		ps rms
Out-of-Range Recovery Time [1]		12		clocks
SIGNAL-TO-NOISE-AND DISTORTION RATIO [3]				
205 MSPS, FIN = 95 MHz		54.8		dBFS
186 MSPS, FIN = 65 MHz		56		dBFS
SPURIOUS FREE DYNAMIC RANGE [4]				
205 MSPS, FIN = 95 MHz		68		dBc
186 MSPS, FIN = 65 MHz		72		dBc
EFFECTIVE NUMBER OF BITS				
205 MSPS, FIN = 95 MHz		8.8		Bit
186 MSPS, FIN = 65 MHz		9		Bit
INTERMODULATION DISTORTION [5]				
205 MSPS, FIN = 99 & 101 MHz		69		dBc
205 MSPS, FIN = 200 & 202 MHz		63		dBc
205 MSPS, FIN = 300 & 303 MHz		59		dBc

1. The time required for the ADC to return to specified characteristics after an out-of-range sample.
2. The SNR is the rms ratio of the measured input signal to the sum of all other spectral components excluding the dc and the first eight harmonics.
3. The SNDR is the rms ratio of the measured input signal to the sum of all other spectral harmonics excluding the dc component
4. The SFDR is the amplitude difference between the measured input signal and the highest harmonic component.
5. The IMD is the rms ratio between the sum of the input signals and the highest harmonic component.

6.4.3 Dual 12-bit DAC (Baseband)

The PVG610A has a dual channel DAC. It uses a segmented current source architecture to provide 12-bit dynamic performance with update rates up to 200 MSPS. The core includes edge-triggered input latches, an internal voltage reference and bias circuitry that include 3-bits programmable, full-scale, output current from 4 to 20 mA. The complementary current outputs support a differential output swing of up to 1.5 V peak-to-peak. The DAC is used in direct IF or in IQ modes.

The following pins are used when using the internal DAC:

DAC_CLK_N/P	DAC clock input. LVPECL levels
OUT_I/Q_N/P	differential Analogs
DAC_CLK_VDD1P2 DAC_CLK_VSS	1.2 V voltage supply and ground for the DAC clock network
DAC_VDD1P2	1.2 V voltage supply for the DAC core
DAC_VDD3P3	3.3 V voltage supply for the DAC output stage
DAC_VSS	ground pin for the core and output stage supplies
IREF	When using the internal DAC, IREF has to be connected to an external resistor (8.2 kohm +/-1%). Otherwise IREF can remain unconnected or connected (whichever is more convenient to the board designer)

For low performance application a single ended clock may be used as the DAC's clock. This clock is transferred into the PVG610A via SPARE2 pin.

The following figure illustrates an example for DAC output connection.

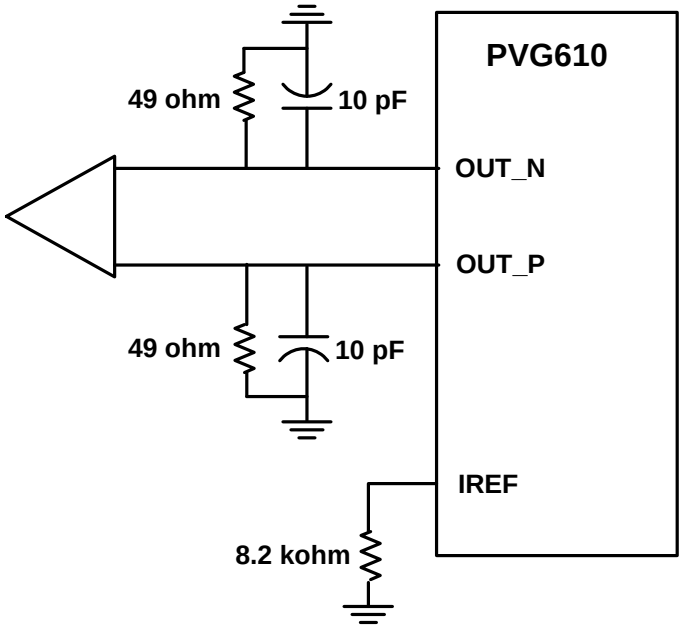


Figure 102: DAC Differential Connection

6.4.3.1 DC Specifications

(At TA = 25 ºC, VAVDD1V2 =1.2V, VAVDD3V3 = 3.3 V, FCLK = 160 MHz, IFS = 10 mA, FOUT = 10 MHz, 1.0 Vp-p differential output swing, data per channel unless otherwise specified)

Table 49: Dual DAC DC Specifications

Parameter (condition)	Min	Typ	Max	Units
DC accuracy				
Resolution	12			Bits
No Missing Codes Guarantied	12			Bits
Monotonicity	Guaranteed			
Integral Non Linearity [1]		± 2.5	± 2.5	LSB
Differential Non Linearity [2]		± 1.5	± 1.5	LSB
Analog Output				
Full-scale Output Current (IFS)	4		20	mA
Single Ended Output Compliance Range	0	0.75	1	V
Differential Output Swing	0.5	1.0	1.5	Vpp
Offset Error (excluding load resistor mismatch) [3]		± 0.05	± 0.1	% of FSR
Gain Error [4]			± 6.5	% of FSR
Gain Matching between ch 0 and 1, (± 1 sigma)		± 0.25		% of FSR
Reference Voltage				
Reference Voltage	1.19	1.24	1.32	V

1. Integral Non Linearity is the deviation of the DAC transfer function from the ideal transfer function. The ideal transfer function is defined as a straight line between the end points of the transfer characteristic corrected for gain and offset. INL for each code is calculated at the code transitions.
2. In an ideal DAC every code transition to its neighbors equals 1 LSB. DNL is the deviation of each code transition from the ideal value.
3. Mid output ideally occurs for mid code input. The offset error is the difference of the actual output at mid code input and the ideal mid output.
4. The deviation of the actual difference between the first and last code transition and the ideal difference.

6.4.3.2 Dynamic Specifications

(At TA = 25 ºC, VAVDD1V2 =1.2V, VAVDD3V3 = 3.3 V, FCLK = 160 MHz, IFS = 10 mA, FOUT = 10 MHz, 1.0 Vp-p, Output Common Mode = 0.25V, differential output swing, data per channel unless otherwise specified)

Table 50: Dual DAC Dynamic Specifications

Parameter (condition)	Min	Typ	Max	Units
Switching performance				
Update Rate	0		200	MSPS
OUTPUT NOISE [1]				
I_{FSR} = 20 mA, 100Hz – 2G Hz		100		pA / $Hz^{½}$
I_{FSR} = 20 mA, 100Hz – 160MHz		200		pA / $Hz^{½}$
I_{FSR} = 10 mA, 100Hz – 2GHz		40		pA / $Hz^{½}$
I_{FSR} = 10 mA, 100 Hz – 160MHz		140		pA / $Hz^{½}$
spurious free dynamic range [2]				
160 MSPS, 10 mA IFS, FOUT = 9 MHz, 0dBFS		78.5		dBc
160 MSPS, 10 mA,IFS, FOUT = 29 MHz		74.7		dBc
187 MSPS, 10 mA IFS, FOUT = 140 MHz, 0dBFS		60.4		dBc
channel isolation				
160 MSPS, 10 mA IFS, FOUT = 10 MHz		72		dBc
160 MSPS, 10 mA IFS, FOUT = 30 MHz		70		dBc
Two TONE INTERMODULATION				
80 MSPS, FOUT1,2 = 9.5, 10.5 MHz		72		dBc
80 MSPS, FOUT,2 = 19, 20 MHz		70		dBc
CHANNEL MISMATCH				
Gain at 80 MSPS, FOUT = 30 MHz		0.1		dBc
Phase at 80 MSPS, FOUT = 30 MHz		0.2		degrees

1. Output noise density with a DC signal input.
2. SFDR is the amplitude difference between the measured output signal and the highest harmonic component.

6.4.4 Envelope 10-bit ADC

The PVG610A has an internal envelope detector, ADC operating at up to 80 MHz. The clock is generated internally with the option of divide by 1, 2 or 4 from the DAC clock.

The following pins are used with the ADC:

ENV_IN_N/P

ENV_VCM

The envelope detector ADC is sharing the DC core voltage of the DAC source. Thus, DAC_VDD1P2 and DAC_VSS need to be connected to external DC source when using this ADC.

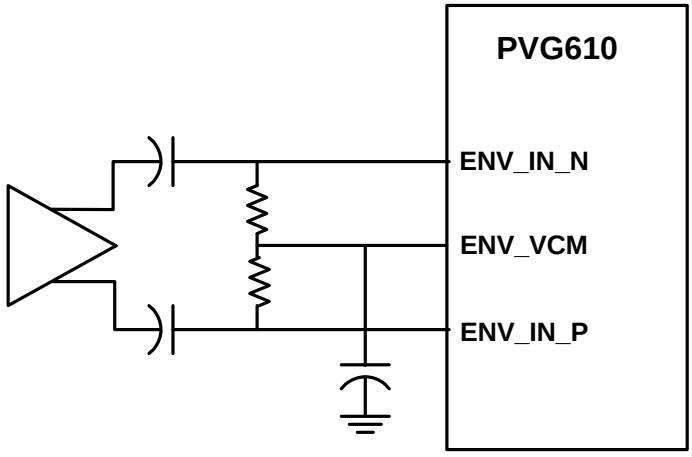


Figure 103: Envelop Detector ADC Connection

6.4.4.1 DC Specifications

(At TA = 25 ºC, VAVDD = 1.2 V, FCLK = 60 MHz, FIN = 10 MHz, internal references, differential full-scale input signal with internal common mode reference and 50 % duty cycle clock unless otherwise specified)

Table 51: Envelop ADC DC Specifications

Parameter (conditions)	Min	Typ	Max	Units
DC ACCURACY				
Resolution (25MSPS to 60MSPS)	10			Bits
No Missing Codes Guaranteed @ 60MSPS	10			Bits
Monotonicity Guaranteed @ 60MSPS	10			Bits
Integral Non Linearity [1]		± 0.3	± 1.5	LSB
Differential Non Linearity [2]		± 0.5	± 1.0	LSB
Gain Error. (3 sigma value) [3]			± 45	mV
Offset Error (one sigma value) [4]			± 5	mV
ANALOG INPUT				
Input Differential Voltage Range		± 0.5		V
Input Capacitance		0.7		pF
Analog Input Bandwidth	0.76	1.1		GHz
VCM output voltage		0.64		V
Max Allowed VCM Current	10			ua
Input signal common mode level	0.50	0.64	0.75	V

1. The deviation of the ADC transfer function from the ideal transfer function. The ideal transfer function is defined as a straight line between the end points of the transfer characteristic corrected for gain and offset. INL for each code is calculated at the code transitions.
2. In an ideal ADC the difference between every code transition and its neighbors equals 1 LSB. DNL is the deviation between each code transition and the ideal value.
3. The deviation of the actual difference between the first and last code transition and the ideal difference.
4. Mid code ideally occurs for zero differential input. The offset error is the differential input voltage that gives mid code.

6.4.4.2 Dynamic Specifications

(At TA = 25 ºC, VAVDD = 1.2 V, FCLK = 60 MHz, FIN = 10 MHz, internal references, differential full-scale input signal with internal common mode reference and 50 % duty cycle clock unless otherwise specified)

Table 52: Envelop ADC Dynamic Specifications

Parameter (condition)	Min	Typ	Max	Units
switching performance				
Conversion Rate	8		80	MSPS
Input Clock Duty Cycle	20		80	%
Aperture Uncertainty (Jitter)		1.0		ps rms
Out-of-Range Recovery Time		2		clocks
SIGNAL-TO-NOISE-AND DISTORTION RATIO				
57 MSPS, FIN = 10.7 MHz		55.8		dBFS
Spurious free dynamic range				
57 MSPS, FIN = 10.7 MHz		71		dBc
effective number of bits				
57 MSPS, FIN = 10.7 MHz		9		Bit

6.4.5 DC Correction

The DC correction interface is used for DC cancellation for the baseband signal before entering the DAC. The PVG610A transfers 16 bits correction words through the DC_COR_I and DC_COR_Q signals. An external DC cancellation device mechanism translates these words into analog levels (I and Q) which are then fed into the analog driver which feeds the DAC.

6.4.5.1 AC Characteristics

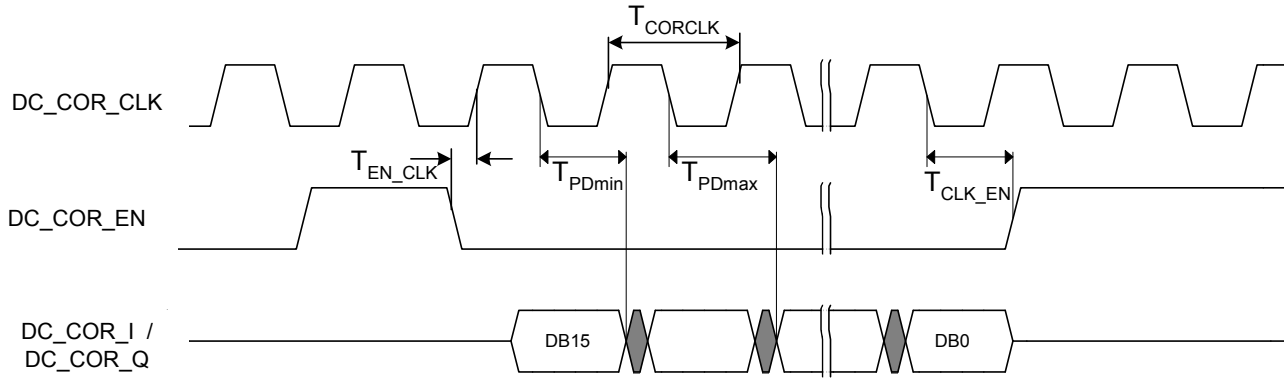


Figure 104: DC Correction Timing

Table 53: DC Correction - AC Characteristics

Parameter	Symbol	Min	Max	Units	
DC_COR_CLK Period	T_{CORCLK}	50		ns	
DC_COR_EN low to rising edge of DC_COR_CLK	T_{EN_CLK}	0		ns	
Falling edge of DC_COR_CLK to DC_COR_EN high	T_{CLK_EN}	4.5		ns	
DC_COR_EN High time	T_{EN_H}	55		ns	
Falling edge of DC_COR_CLK to DC_COR_I / DC_COR_Q propagation delay	T_{PD}	5.5	37.5	ns	relative to falling edge

6.4.6 Receive External ADC

The user may choose to use external ADC's instead of the integrated ADC's in the PVG610. The ADC Bypass interface consists of two 12-bits data input buses and an input clock. The maximum clock rate is 100MHz.

In order to support IF sampling, at frequency higher than 100MHz, two samples can be taken-in at any clock rising edge using the I and Q data buses (the earlier sample can be connected to I or Q bus as configured by the configuration file).

The external dual-ADC can be connected to one of two following sets of pins:

INJCT_I_ADC_A[11:0], INJCT_Q_ADC_B[11:0], INJCT_STB_ADC_CLKIN

INJCT2_I_ADC2_A[11:0], INJCT2_Q_ADC2_B[11:0], INJCT2_STB_ADC2_CLKIN

Note that each of the sets shares pins with other interfaces. The first set shares pins with Injection bus 1, DAC Bypass and SDRAM signals. The second set shares pins with MII and STM signals.

6.4.6.1 AC Characteristics

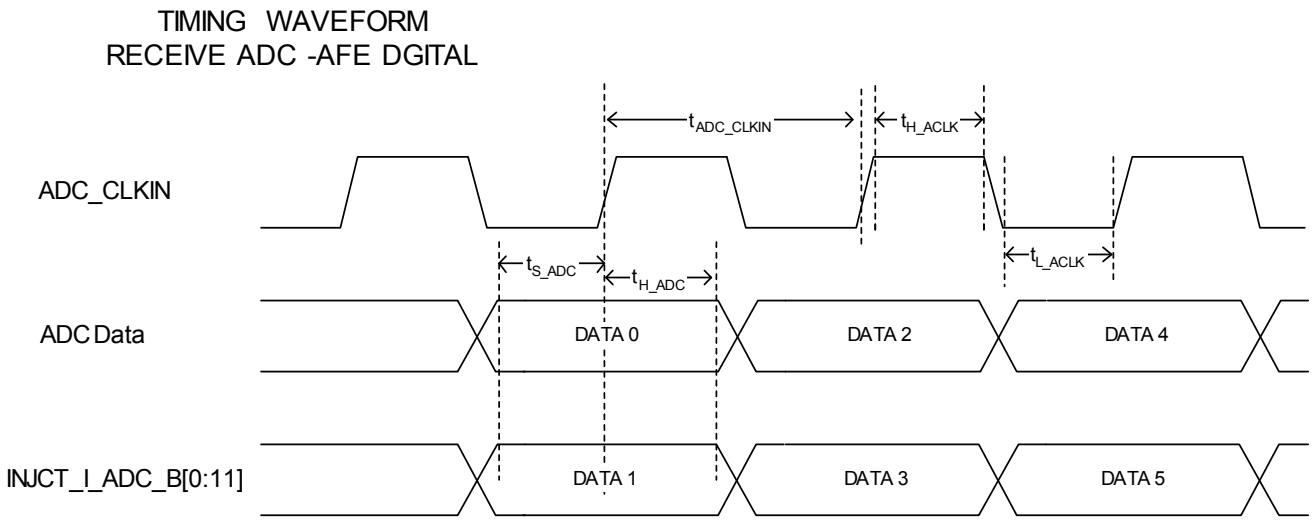


Figure 105: Receive External ADC Timing

Table 54: Receive External ADC - AC Characteristics

Parameter	Symbol	Min	Typ	Max	Units
ADC_CLKIN clock period	t_{ADC_CLK}	10			ns
ADC_CLKIN high	t_{H_ACLK}		50		ns
ADC_CLKIN low	t_{L_ACLK}		50		ns
ADC data* setup time in respect to ADC_CLKIN	t_{S_ADC}	1.3-0.5= 0.8 INJC1 = 1.5 INJC2 = 0.5			ns
ADC data* hold time in respect to ADC_CLKIN	t_{H_ADC}	2-0.5= 1.5 INJC1 = 0.5 INJC2 = 3.6			ns

*ADC Data: INJCT_I_ADC_A [0:11], INJCT_Q_ADC_B [0:11],
INJCT2_I_ADC2_A [0:11], INJCT2_Q_ADC2_B [0:11]

6.4.7 Transmit External DAC

The user may choose to use external DAC's instead of using the integrated DAC's in the PVG610. The DAC Bypass interface consists of two 12-bits data output buses (DAC_I[11:0] and DAC_Q[11:0]). The clock signal is the one used for the internal DAC (the LVPECL DAC_CLK signal or the single ended SPARE2 signal). The maximum supported clock frequency when using the DAC bypass mode is 100MHz.

In order to support IF sampling, at frequency higher than 100MHz, two samples can be taken at any clock rising edge using the I and Q data buses (the earlier sample can be connected to I or Q bus as configured by the configuration file).

6.4.7.1 AC Characteristics

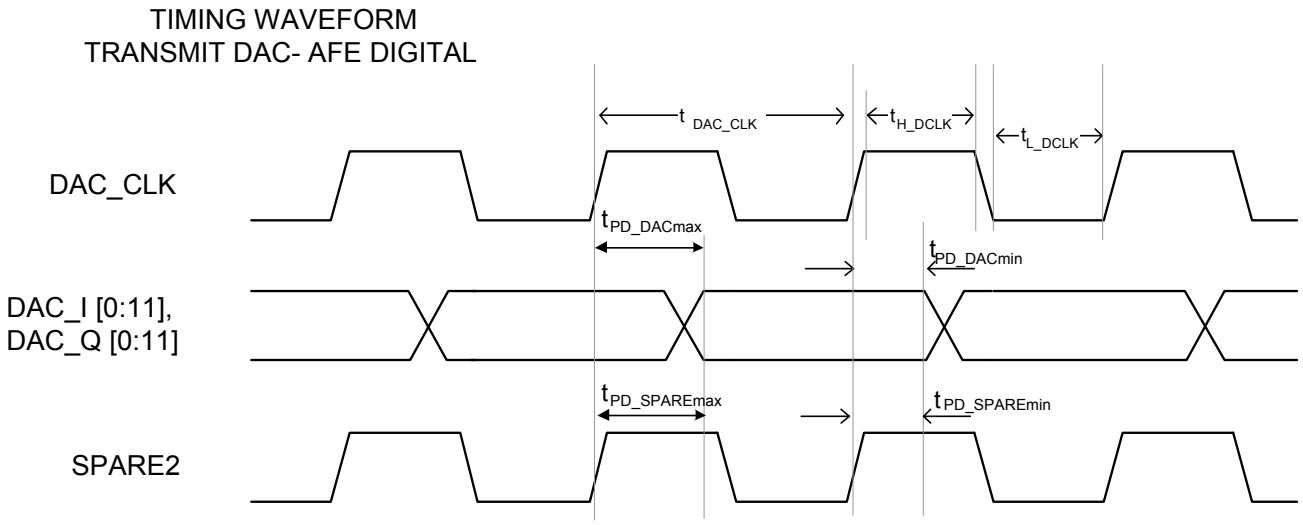


Figure 106: Transit External DAC Timing

Table 55: Receive External DAC AC Characteristics

Parameter	Symbol	Min	Typ	Max	Units
DAC_CLK clock period	t_{DAC_CLK}	10			ns
DAC_CLK high	t_{H_DCLK}		50		ns
DAC_CLK low	t_{L_DCLK}		50		ns
DAC_I [0:11], DAC_Q [0:11] output propagation delay in respect to DAC_CLKIN	t_{PD_DAC}	3.55		9	ns
DAC_I [0:11], DAC_Q [0:11] output propagation delay in respect to SPARE2	t_{PD_SPARE2}	3		8	ns

6.5 Protection Interface

When configured as a Working board the PVG610A uses TXP_OUT and RXP_IN as transmit and receive signals.

When configured as a Protection board the PVG610A uses TXP_IN and RXP_OUT as transmit and receive signals. The following drawings illustrate two connection alternatives between Working and Protection boards: A parallel protection bus transferred between the boards is shown in the first drawing. Connecting the data between the Working and Protection PVG610A via SERDES devices are shown in the second drawing.

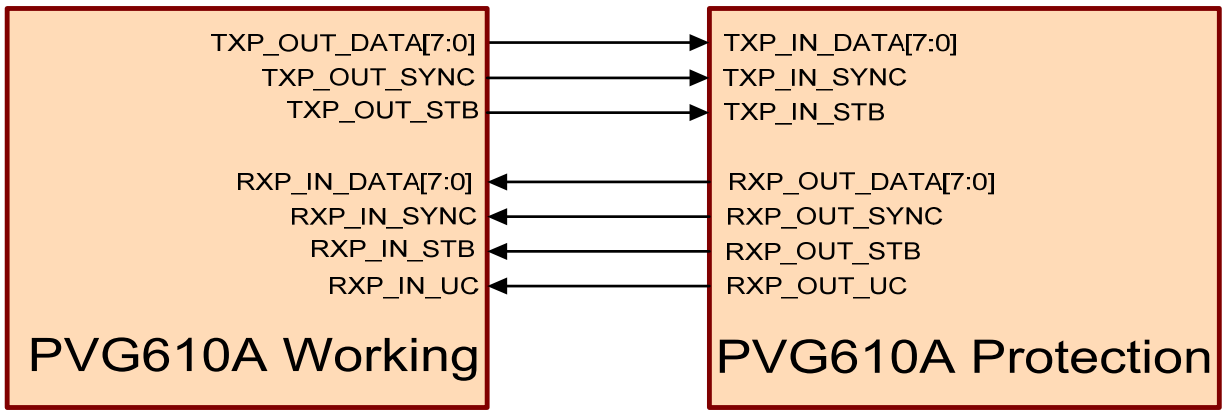


Figure 107: Connecting Protection System with Parallel Protection Bus

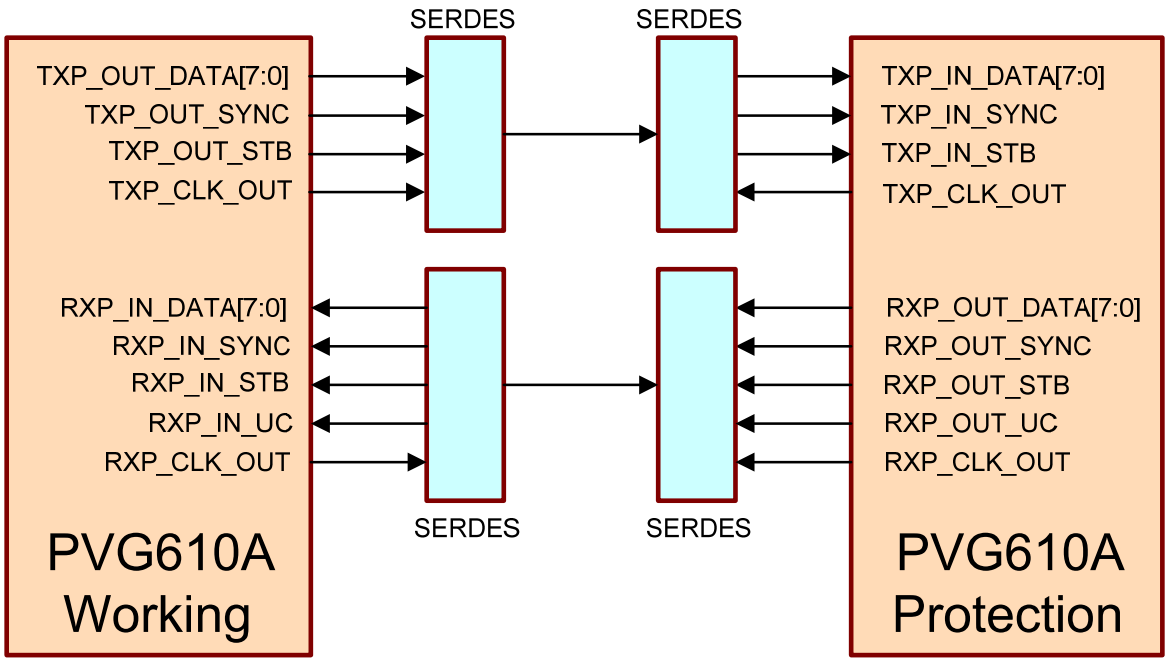
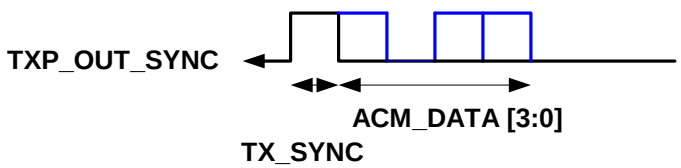


Figure 108: Connecting Protection System with SERDES Devices

TXP_DATA[7:0] data is transferred from the working framer to the protection modem. The air frame synchronization pulse and the four-bits ACM profile are mixed in a serial signal (TXP_SYNC) as follows:



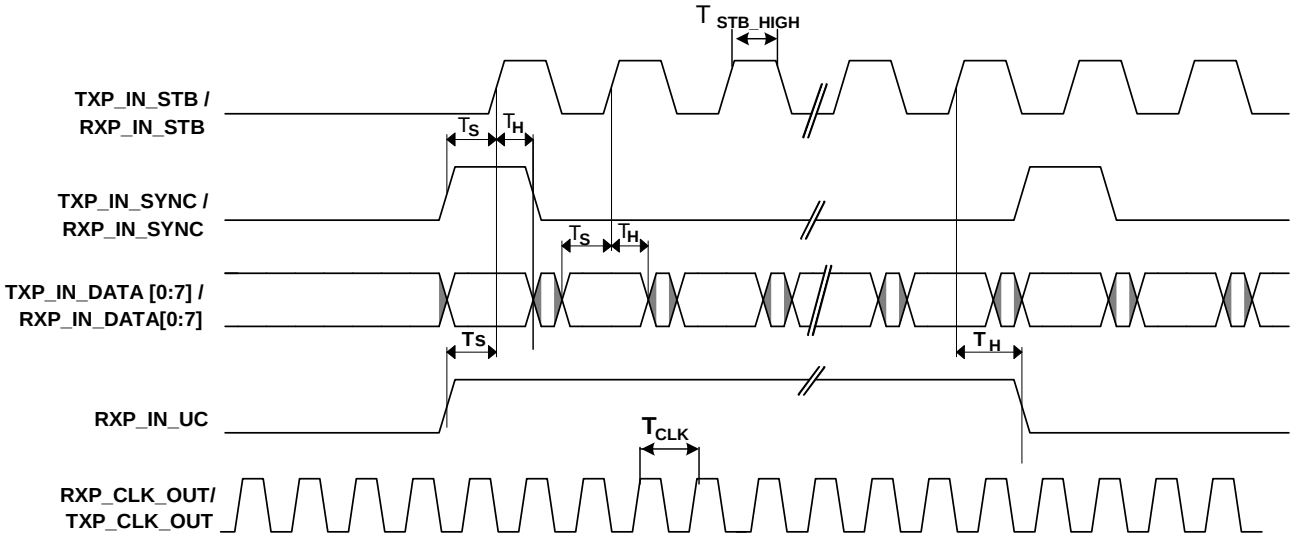
The TXP_STB is the clock signal according to which TXP signals are sampled in/out. The STB frequency is up to 50Mhz and is set according to the configuration parameters. The TXP_STB contains silence periods when there are no valid bytes to transfer.

RXP_DATA[7:0] data is transferred from the protection modem to the working framer. The air frame pulse and the four-bits ACM profile are mixed in a serial signal (RXP_SYNC) in the same way as in TXP_SYNC signal. RX_UC signal transfers indication whether the data is OK. When air loss occurs, or when the data is part of an erroneous decoded FEC block, RX_UC signal is high. The RXP_STB is the clock signal according to which RXP signals are sampled in/out. The STB frequency which is up to 50Mhz is set according to the configuration parameters and. RXP_STB contains silence periods when there are no valid bytes to transfer.

TXP_IN and TXP_OUT signals share the same pins and change functionality/direction according to the board role (Protection or Working). The same applies for RXP_IN and RXP_OUT. During reset all signals are set as input signals. In order to prevent bus contention (when changing the roles of the boards) it is recommended to use HW protection means on the PCB between the Working and Protection PVG610's (e.g. serial resistors).

When connecting the Working and Protection boards via serial links (with SERDES devices) all of the protection-bus signals are sampled in or out of the PVG610A with TXP_CLK_OUT and RXP_CLK_OUT signals. These clock signals run at half the system clock rate.

6.5.1.1 Protection AC Characteristics



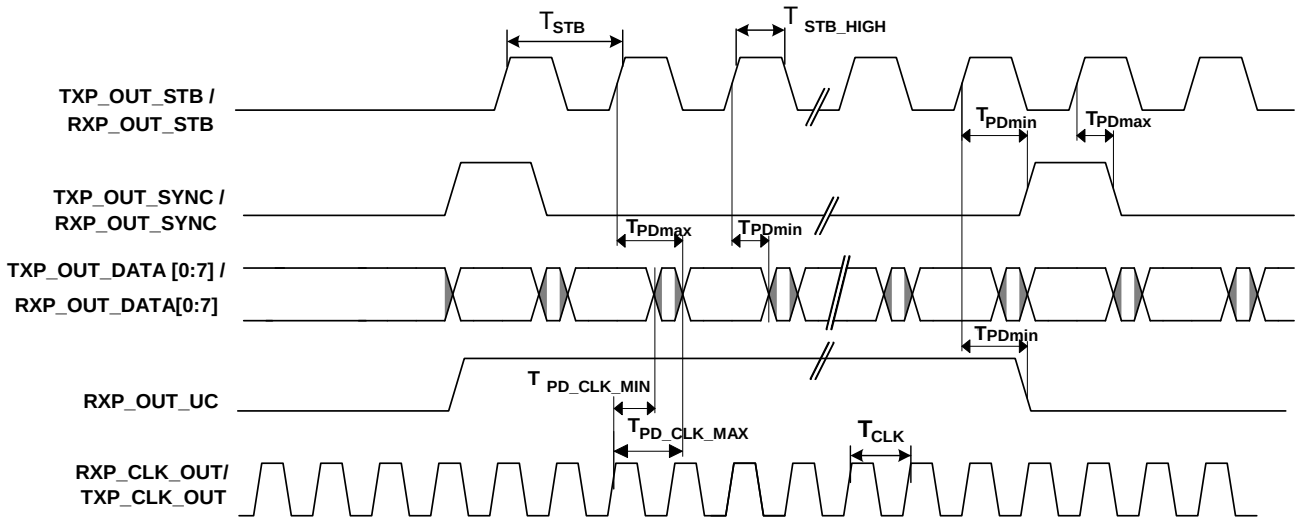


Figure 109: Protection Bus Timing Diagrams

Table 56: Protection Interface Timing

Parameter	Symbol	Min	Max	Units
PVG610A IN				
TXP_IN_STB / RXP_IN_STB Strobe high time	T_{STB_HIGH}	$2*t_{SYS}$		ns
TXP_IN_STB / RXP_IN_STB Strobe cycle period	T_{STB}	$4*t_{SYS}$		ns
TXP_IN_DATA, IN_SYNC, IN_UC setup time in respect to IN_STB rising edge	T_S	1		ns
TXP_IN_DATA, IN_SYNC, IN_UC hold time in respect to IN_STB rising edge	T_H	0.5		ns
PVG610A OUT				
TXP_OUT_STB / RXP_OUT_STB Strobe high time	T_{STB_HIGH}	$2*t_{SYS}$		
TXP_OUT_STB / RXP_OUT_STB Strobe cycle period	T_{STB_P}	$4*t_{SYS}$		
TXP_OUT_DATA, OUT_SYNC, OUT_UC propagation delay in respect to OUT_STB rising edge	T_{PD}	9.5	10.5	ns
RXP/TXP_OUT_DATA, OUT_SYNC, OUT_UC propagation delay in respect to TXP_CLK_OUT rising edge	T_{PD_CLK}	0	2.5	ns
RXP_CLK_OUT/ TXP_CLK_OUT cycle period	T_{CLK}	$2*t_{SYS}$	$2*t_{SYS}$	

6.6 XPIC Interface

The following figure illustrates the use of the XPIC interfaces.

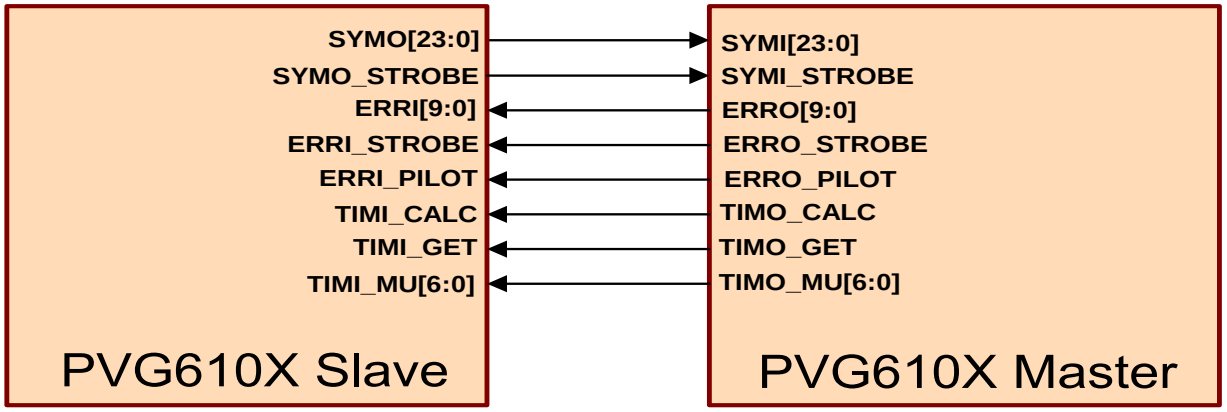
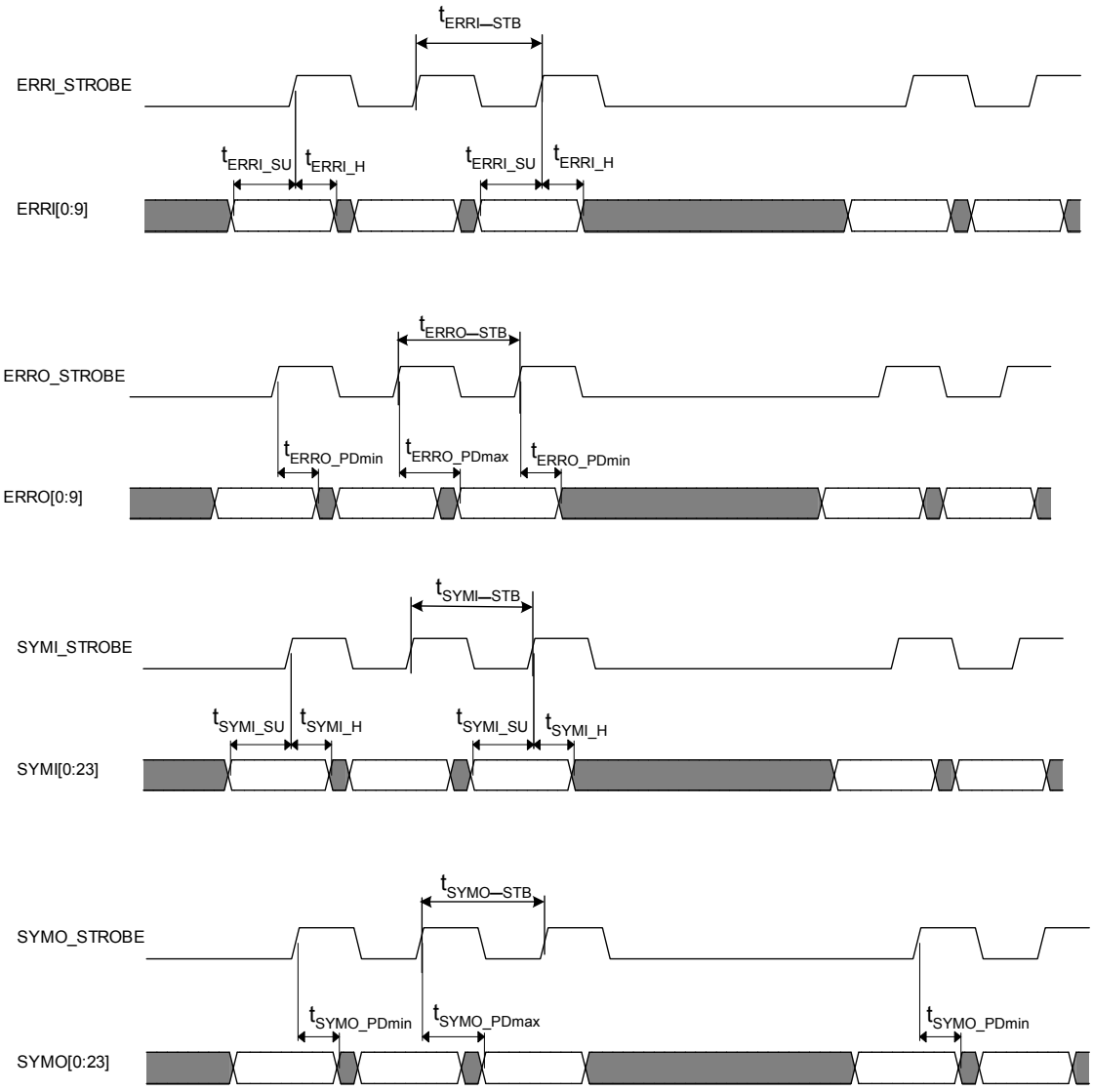


Figure 110: Using XPIC Interface in XPIC Configuration

6.6.1.1 AC Characteristics



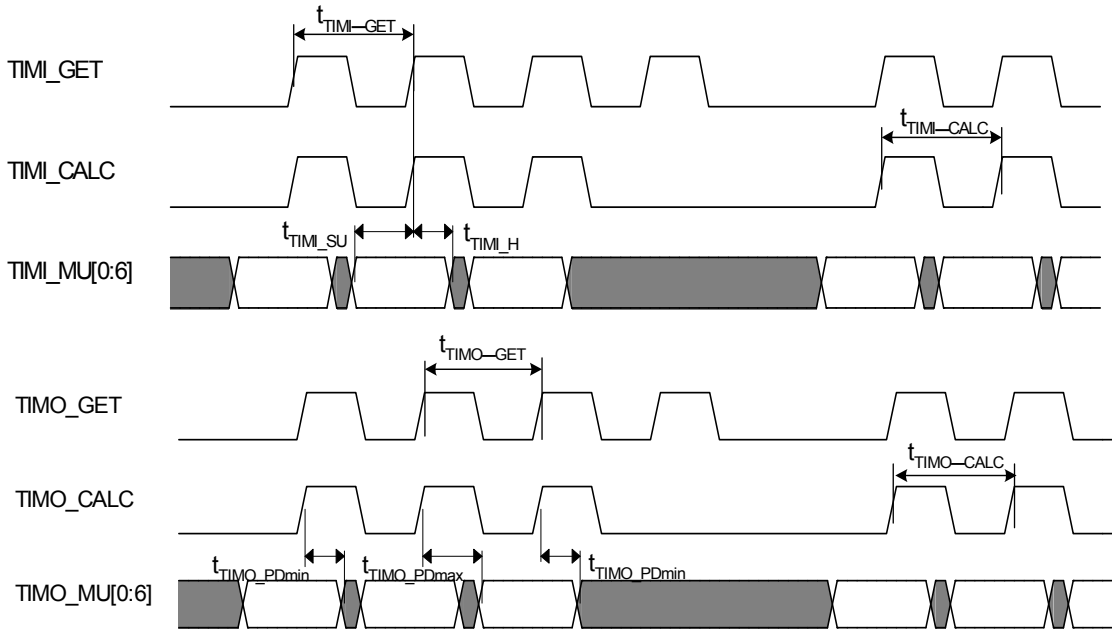


Figure 111: XPIC Interface Timing Diagrams

Table 57: XPIC Transmit Data Timing

Parameter	Symbol	Min	Max	Units	Remarks
ERRO_STROBE period	t_{ERRO_STB}	20		ns	
ERRO[0:9] propagation delay in respect to ERRO_STROBE rising edge	t_{ERRO_PD}	9	11	ns	
SYMO_STROBE period	t_{SYMO_STB}	20		ns	
SYMO[0:23] propagation delay in respect to SYMO_STROBE rising edge	t_{SYMO_PD}	9	11	ns	
TIMO_GET period	t_{TIMO_GET}	10		ns	
TIMO_CALC period	t_{TIMO_CALC}	10		ns	
TIMO_MU [0:6] propagation delay in respect to TIMO_GET rising edge		4.5	5.5	ns	

Table 58: XPIC Receive Data timing

Parameter	Symbol	Min	Max	Units	Remarks
ERRI_STROBE period	t_{ERRI_STB}	20		ns	
ERRI_[0:9] setup time in respect to ERRI_STROBE	t_{ERRI_SU}	3		ns	
ERRI_[0:9] HOLD time in respect to ERRI_STROBE	t_{ERRI_H}	8		ns	
SYMI_STROBE period	t_{SYMI_STB}	20		ns	
SYMI[0:23] setup time in respect to SYMI_STROBE	t_{SYMI_SU}	3		ns	
SYMI[0:23] hold time in respect to SYMI_STROBE	t_{SYMI_H}	8		ns	
TIMI_GET period	t_{TIMI_GET}	10		ns	
TIMI_CALC period	t_{TIMI_CALC}	10		ns	
TIMI[0:6] setup time in respect to TIMI_GET	t_{TIMI_SU}	2		ns	
TIMI[0:6] hold time in respect to TIMI_GET	t_{TIMI_H}	4		ns	

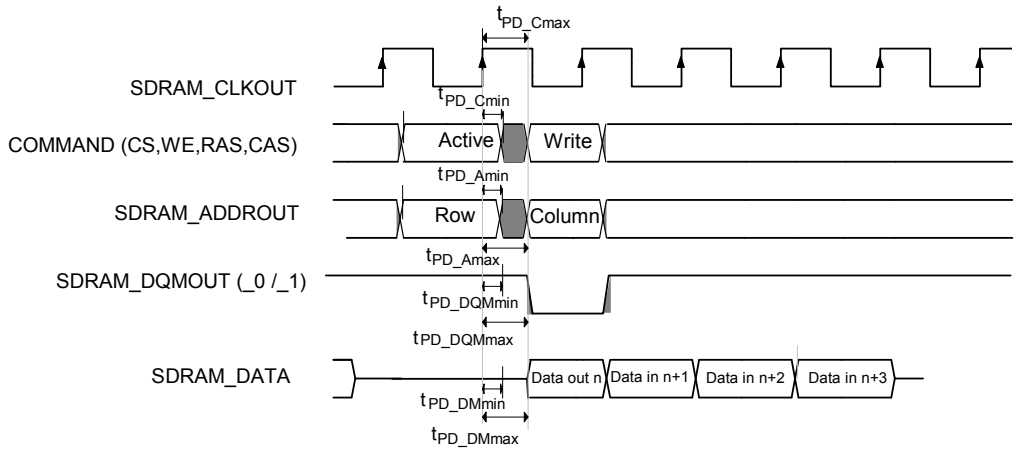
6.7 Infrastructure Interfaces

6.7.1 SDRAM Interface

The PVG610A support the connection of 64Mbyte SDRAM. A 16bits data bus is used. The maximum clock frequency is 100MHz. The SDRAM interface is compliant to standard SDRAM devices.

6.7.1.1 SDARM AC Characteristics

Write:



Read

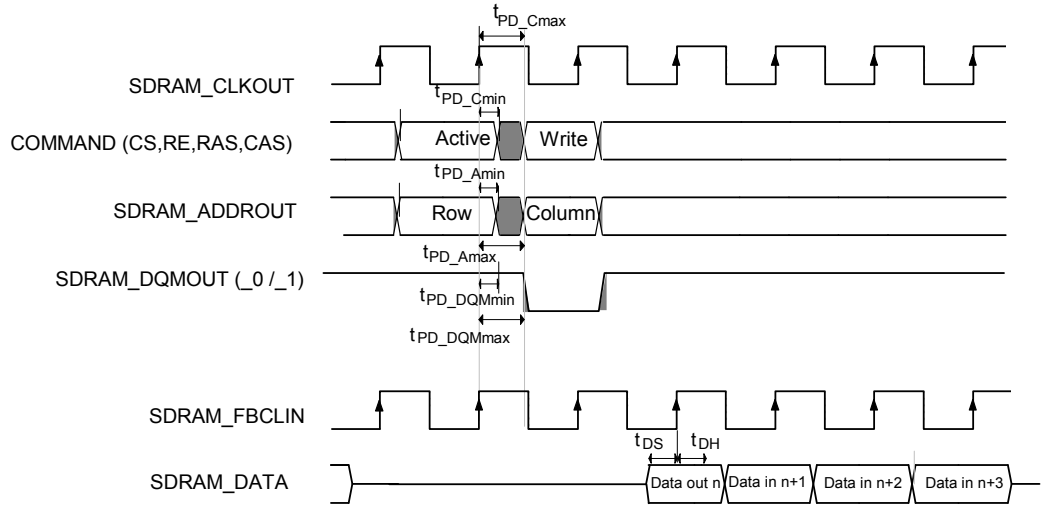


Table 59: SDRAM Interface AC Characteristics

AC Characteristics Parameter	Symbol	Min	Typ	Max	Units	Remarks
SDRAM_CLKOUT to Command CS Propagation Delay	t_{PD_CS}	0.8		3.6	ns	
SDRAM_CLKOUT to Command WE Propagation Delay	t_{PD_WE}	1.8		5.3	ns	
SDRAM_CLKOUT to Command RAS Propagation Delay	t_{PD_RAS}	0.25		2.3	ns	
SDRAM_CLKOUT to Command CAS Propagation Delay	t_{PD_CAS}	1.9		6.29	ns	
SDRAM_CLKOUT to SDRAM_ADDROUT Propagation Delay	t_{PD_A}	2.7		5	ns	
SDRAM_CLKOUT to SDRAM_DQMOUT_0 / SDRAM_DQMOUT_0 Propagation Delay	t_{PD_DQM}	1.8		5.3	ns	
SDRAM_DATA Setup Time in respect to SDRAM_FBCLKIN	t_{DS}	1.5			ns	
SDRAM_DATA Hold Time in respect to SDRAM_FBCLKIN	t_{DH}	1.5			ns	
SDRAM_CLKOUT to SDRAM_DATA Propagation Delay	t_{PD_D}	0.75		5.9	ns	

6.8 Test and Diagnostics Interfaces

6.8.1 JTAG

The PVG610A contains JTAG interface. This interface is used for a boundary scan or for software debug. JTAG_SEL input signal selects one of these two options (‘0’ for boundary scan and ‘1’ for software debug).

Software debug is performed by connecting Multi-ICE or RealView-ICE to the internal ARM processor via the JTAG interface. The RTCK signal supports adaptive clocking mode for Multi-ICE or RealView-ICE, when the ICE is configured in adaptive clocking mode. Adaptive clocking ensures that the TCK is sufficiently slow to work with a synthesizable core and that its frequency is near the maximum rate possible. In most cases, adaptive clocking is not required (it is only required to set up TCK with a frequency sufficiently slow). Nevertheless, adaptive clocking is necessary when debugging a target with variable clock speed.

6.8.1.1 JTAG AC Characteristics

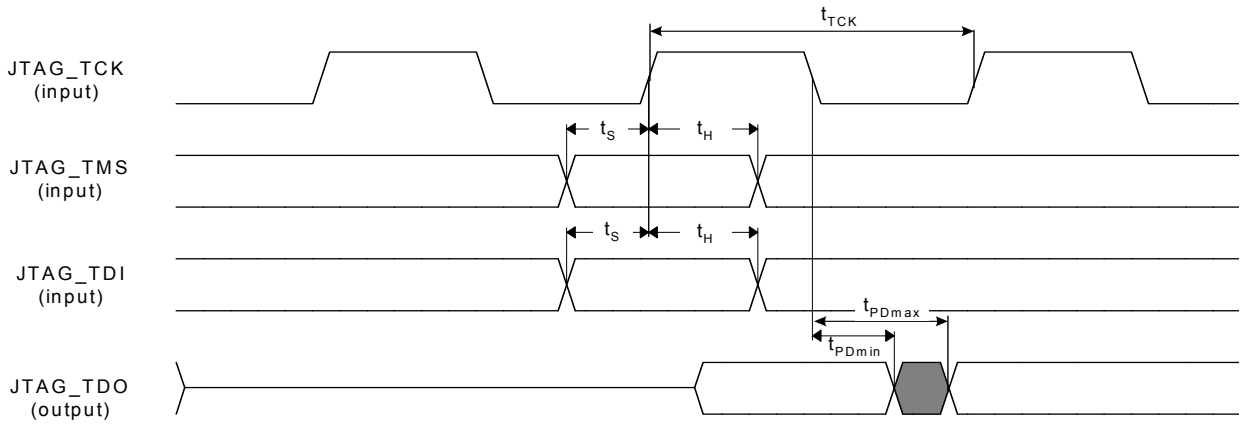


Figure 112: JTAG Timing

Table 60: JTAG AC Characteristics

Parameter	Symbol	Min	Max	Units	Remarks
JTAG_TCK period	t_{TCK}	25		ns	
JTAG_TMS / JTAG_TDI to JTAG_TCK rising edge setup time	t_S	10		ns	relative to rising edge
JTAG_TCK rising edge to JTAG_TMS / JTAG_TDI hold time	t_H	10		ns	relative to rising edge
JTAG_TCK falling edge to JTAG_TDO propagation delay	t_{PD}	50	60	ns	relative to falling edge

6.8.2 Injection Bus

The Injection Bus can be used to inject data into one of five points in the MODEM receive path. The following figure illustrates the supported injection points.

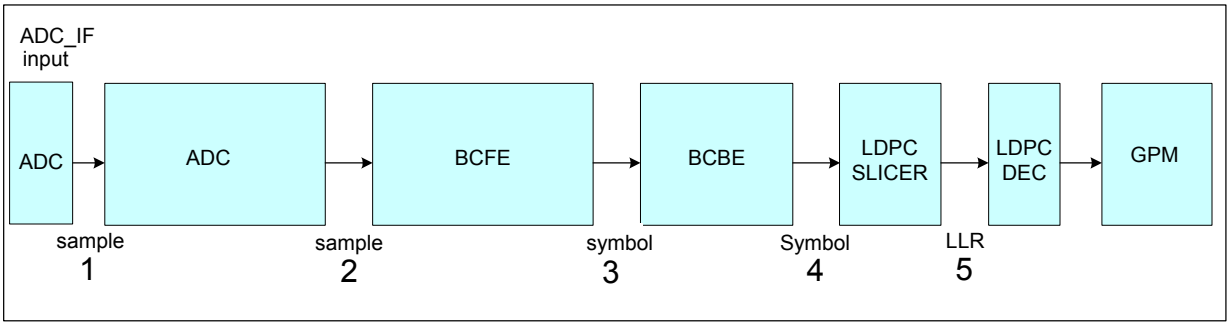


Figure 113: Injection bus diagram

The user can choose one of two available sets of pins through which the data can be injected (the two sets are referred to as INJCT and INJCT2). The Injection Bus consists of 24 data lines, 5 control lines and a strobe signal. The control bits specify the type of data transferred over the data line. The strobe signal is used to sample the data and control signals, into the PVG610.

6.8.2.1 AC Characteristics

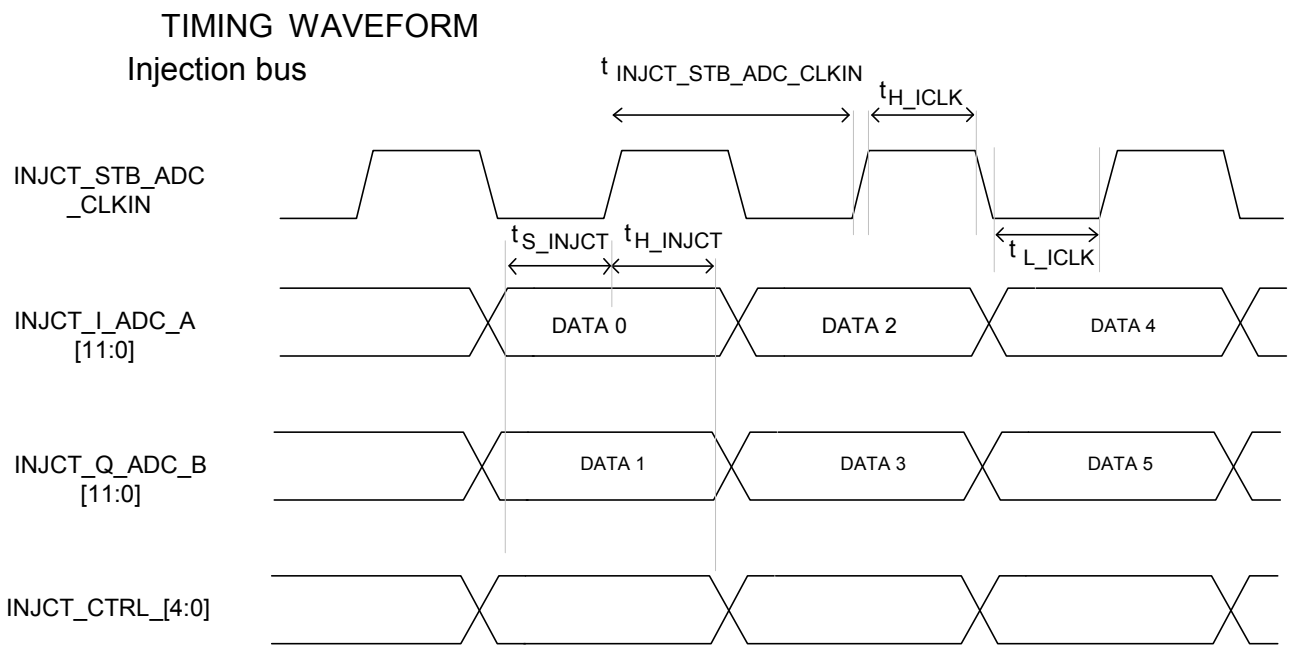


Figure 114: Injection BUS Timing

Table 61: Injection BUS AC Characteristics

Parameter List	Symbol	Min	Typ	Max	Units
INJCT_STB_ADC_CLKIN clock period	$t_{INJCT\_STB\_ADC\_CLKIN}$	10			ns
INJCT_STB_ADC_CLKIN high	t_{H_ICLK}		TBD		ns
INJCT_STB_ADC_CLKIN low	t_{L_ICLK}		TBD		ns
INJCT data* setup time in respect to INJCT_STB_ADC_CLKIN	t_{S_INJCT}	1.3-0.5= 0.8			ns
INJCT data* hold time in respect to INJCT_STB_ADC_CLKIN	t_{H_INJCT}	2-0.5= 1.5			ns

* INJCT Data : INJCT_I_ADC_A [0:11] , INJCT_Q_ADC_B [0:11], INJCT_CTRL [4:0], INJCT2_I_ADC2_A [0:11] , INJCT2_Q_ADC2_B [0:11] , INJCT2_CTRL [4:0]

6.8.3 Test Bus

The test bus consists of 31 data lines and a bus strobe (TEST_31). Data lines are sampled on the rising edge of the strobe signal (TEST_31).

6.8.3.1 AC Characteristics

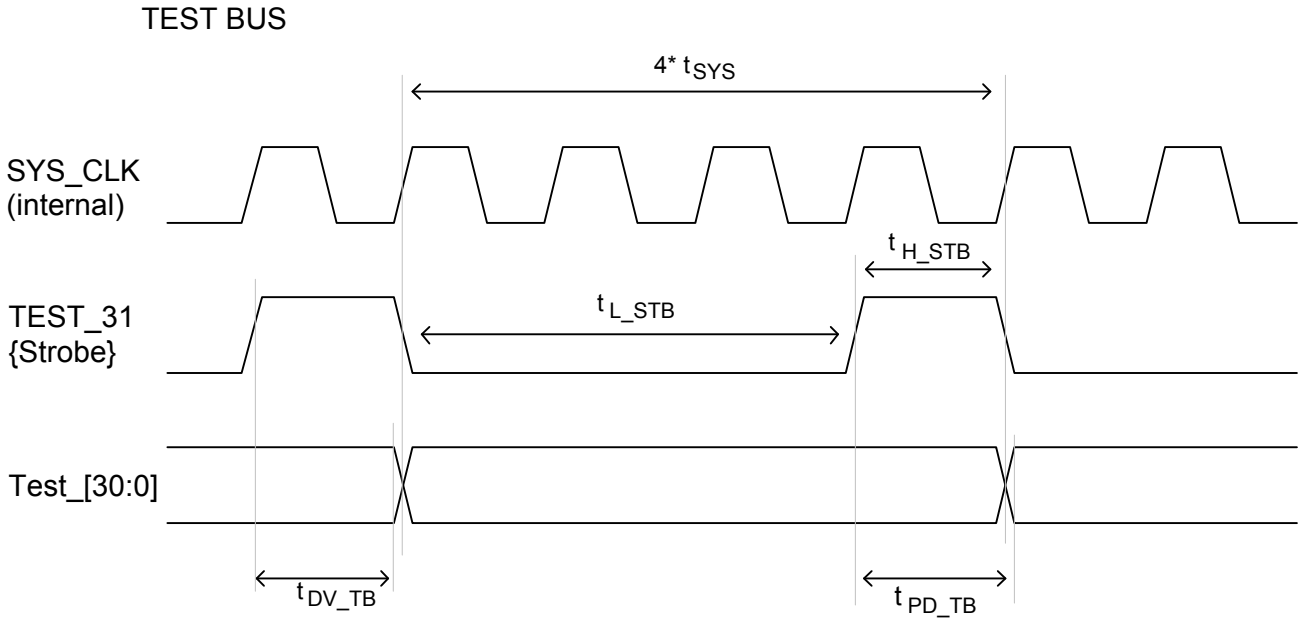


Figure 115: Test BUS Timing

Table 62: Test Bus Timing Parameters

Parameter	Symbol	Min	Typ	Max	Units
Strobe high	t_{H_STB}	3	t_{SYS}		ns
Strobe low	t_{L_STB}	18	$3*t_{SYS}$		ns
Test Bus data valid	t_{DV_TB}	4			ns
Test Bus propagation delay	t_{PD_TB}			t_{SYS}	ns

7 Performance Characteristics

7.1 BER Vs SNR for AWGN Channels

7.1.1 LDPC

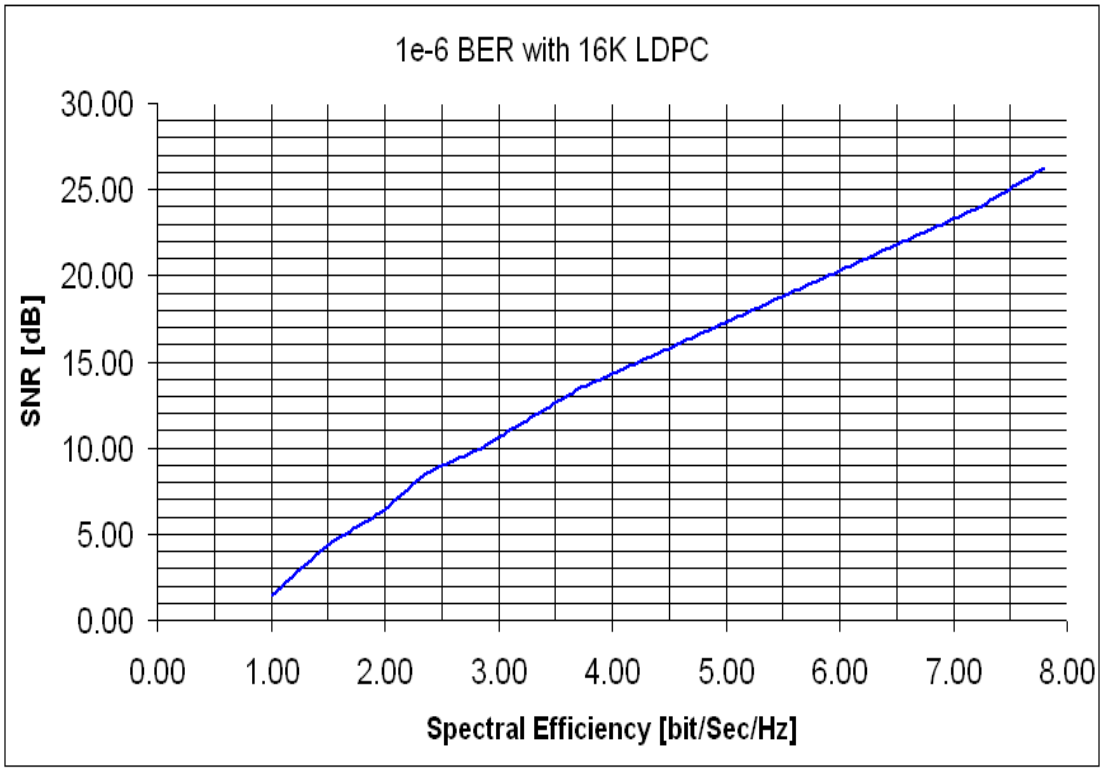


Figure 116: SNR for 1E-6 BER as a function of spectral efficiency (Based on simulations)

The chart above describes the SNR required to achieve BER of 1E-6 with LDPC block size of 16k. For a lower BER or shorter LDPC blocks, a correction factor as detailed in the table below has to be applied to the above chart (shifting the curve upward).

Table 63: Correction Factors for Shorter Blocks and Lower BER (dB)

	16k	8k	4k	2k
1e-6	0.0	0.15	0.4	0.7
1e-8	0.1	0.25	0.6	1.15
1e-10	0.2	0.40	0.9	1.70
1e-12	0.4	0.80	1.4	3.5

7.1.2 Uncoded

Table 64: Uncoded BER VS. SNR

Spectral Efficiency		10^{-3}	10^{-6}	10^{-9}
2	QPSK	9.8	13.5	15.6
4	16-QAM	16.6	20.5	22.6
5	32-QAM	19.5	23.5	25.7
6	64-QAM	22.6	26.8	29.1
7	128-QAM	25.6	30.0	32.6
8	256-QAM	29.4	36.0	44.1

7.1.3 PTCM

Table 65: PTCM VS. SNR

Spectral Efficiency		10^{-3}	10^{-6}
3	16-QAM	11.6	13.8
3.5	16-QAM	13.2	14.9
4.5	32-QAM	16.4	18.3
5	64-QAM	18.1	20.5
5.5	64-QAM	19.5	21.4
6	128-QAM	21.2	23.4
6.5	128-QAM	22.6	24.4
7	256-QAM	24.3	26.5
7.5	256-QAM	25.7	27.5

7.1.4 Concatenated

Table 66: Concatenated BER Vs. SNR (up to 24 branches interleaver)

Spectral Efficiency		PTCM	Reed-Solomon	10^{-3}	10^{-6}	10^{-9}
3.2	16-QAM	7/8	(252,232)	12.6	12.9	13.2
5.1	64-QAM	11/12	(204,188)	19.2	19.5	19.8
6.3	128-QAM	13/14	(231,225)	22.6	23.2	23.7

7.2 Interference

7.2.1 Co-Channel Interference

Table 67: Co-Channel Interference

1 dB degradation at 10^{-6} BER	QPSK 16 QAM 32 QAM 64 QAM 128 QAM 256 QAM	21.2 dB 28.0 dB 31.2 dB 34.9 dB 38.1 dB 40.8 dB
3 dB degradation at 10^{-6} BER	QPSK 16 QAM 32 QAM 64 QAM 128 QAM 256 QAM	17.2 dB 24.0 dB 27.2 dB 30.9 dB 34.1 dB 36.8 dB

7.2.2 Adjacent Channel Interference

Table 68: 1st Adjacent Channel Interference

1 dB degradation at 10^{-3} BER	QPSK 16 QAM 32 QAM 64 QAM 128 QAM 256 QAM	-21.5 dB -14.8 dB -11.5 dB -8.7 dB -5.6 dB -2.3 dB
3 dB degradation at 10^{-3} BER	QPSK 16 QAM 32 QAM 64 QAM 128 QAM 256 QAM	-25.5 dB -18.8 dB -15.5 dB -12.7 dB -9.6 dB -6.3 dB
1 dB degradation at 10^{-6} BER	QPSK 16 QAM 32 QAM 64 QAM 128 QAM 256 QAM	-17.8 dB -11.0 dB -7.8 dB -4.1 dB 0.9 dB 1.8 dB
3 dB degradation at 10^{-6} BER	QPSK 16 QAM 32 QAM 64 QAM 128 QAM 256 QAM	-21.8 dB -15.0 dB -11.8 dB -8.1 dB -4.9 dB -2.2 dB

7.2.3 Second Adjacent Channel Interference

Table 69: Second Adjacent Channel Interference

1 dB degradation at 10^{-3} BER	QPSK 16 QAM 32 QAM 64 QAM 128 QAM 256 QAM	-24.5 dB -17.8 dB -14.5 dB -11.7 dB -8.6 dB -5.3 dB
3 dB degradation at 10^{-3} BER	QPSK 16 QAM 32 QAM 64 QAM 128 QAM 256 QAM	-28.5 dB -21.8 dB -18.5 dB -15.7 dB -12.6 dB -9.3 dB
1 dB degradation at 10^{-6} BER	QPSK 16 QAM 32 QAM 64 QAM 128 QAM 256 QAM	-20.8 dB -14.0 dB -10.8 dB -7.1 dB -3.9 dB -1.2 dB
3 dB degradation at 10^{-6} BER	QPSK 16 QAM 32 QAM 64 QAM 128 QAM 256 QAM	-24.8 dB -18 dB -14.8 dB -11.1 dB -7.9 dB -5.2 dB

8 Electrical Characteristics

8.1 Absolute Maximum Rating

Table 70: Absolute Maximum Rating

Symbol	Parameter	Range
V_{DD} 3.3V	3.3V DC Supplies	3.0-3.6 V
Vin 1.2V	1.2V DC Supplies	1.08-1.32 V
I_O	Pin Output Current	100mA
I_{IN}	Pin Input Current	100mA

8.2 Recommended Operating Conditions

Table 71: Recommended Operating Conditions

Symbol	Parameter	Min	Typ	Max	Units
VDD1P2	Digital Core Operating Voltage	1.2*		1.32	V
VDD3P3	Digital I/O Operating Voltage	3.0	3.3	3.6	V
SYS_CLK_VDD1P2	Analog operating voltage for the system clock network	1.15	1.2	1.32	V
PLL_VDDA1P2	Analog operating voltage for the PLL	1.15	1.2	1.32	V
ADC_VDD1P2	Analog core operating voltage for the dual 12 bits and IF 10 bits ADC's.	1.15	1.2	1.32	V
ADC_VDD3P3	Analog operating voltage for the input stages of the dual 12 bits and IF 10 bits ADC's.	3.15	3.3	3.6	V
ADC_CLK_VDD1P2	Analog operating voltage for the clock network of the dual 12 bits and IF 10 bits ADC's.	1.15	1.2	1.32	V
DAC_VDD1P2	Analog operating voltage for the dual DAC core and envelope ADC	1.15	1.2	1.32	V
DAC_VDD3P3	Analog operating voltage for the output stages of the dual DAC	3.15	3.3	3.6	V
DAC_CLK_VDD1P2	Analog operating voltage for the clock network of the dual DAC	1.15	1.2	1.32	V
LIU_VDD3P3	Analog operating voltage for the E1/T1/J1 LIU	3.15	3.3	3.6	V

* For system clock frequencies of 100MHz or less, the minimum voltage level for VDD1P2 is 1.15v.

8.3 Power Up Sequence

Two power sources are required for the PVG610A 1.2 VDC and 3.3 VDC. The 3.3 VDD_DIGITAL has to be applied before the 1.2 VDD_DIGITAL (the time gap between the two should be >0sec).

During power up, the device must be reset by asserting the NRESET signal until all voltage supplies reached the stable level.

In addition, during power up, the JTAG controller must be reset. This can be achieved by setting JTAG_SEL to ‘1’ or setting JTAG_SEL to ‘0’ and JTAG_TRST to ‘0’.

The JTAG reset assertion can end 200ns after the voltage supplies reached a stable level. The reset assertion must end before using the JTAG controller. Failure to reset the JTAG controller may result with occasional failure of the boot process.

8.4 DC Characteristics of Digital I/O Signals

All PVG610A digital I/O signals follow the DC characteristics as described below unless otherwise specified.

Table 72: DC characteristics of digital I/O signals

	Parameter	Min	Nom	Max
V_{IL}	Input Low Voltage	-0.3V		0.8V
V_{IH}	Input High Voltage	2v		5.5V
V_T+[1]	Schmitt trig. Low to High threshold point	1.57V	1.68V	1.74V
V_T-[1]	Schmitt trig. High to Low threshold point	0.97V	1.03V	1.09V
I_I	Input leakage current @V_I=3.3V or 0V			±10µA
I_{OZ}	Tri-state output leakage current @V_O=3.3V or 0V			±10µA
R_{PU}[2]	Pull-up resistor	39 kΩ	55 kΩ	85 kΩ
R_{PD}[3]	Pull-down resistor	45 kΩ	93 kΩ	198 kΩ
V_{OL}	Output low voltage @I_{OL}=2,4, …, 24 mA			0.4V
V_{OH}	Output high voltage @I_{OH}=2,4, …, 24 mA	2.4V		

Notes:

1. Schmitt trigger parameters are relevant for those pins that are specified, in chapters 2.2-2.4, to have Schmitt Trigger (ST) buffer type.
2. Pull-up resistor parameter is relevant for those pins that are specified, in chapters 2.2-2.4, to have Pull-up (PU) buffer type.
3. Pull-down resistor parameter is relevant for those pins that are specified, in chapters 2.2-2.4, to have Pull-down (PD) buffer type.

8.5 Power Consumption

8.5.1 Digital Core

The current consumed by the digital core (VDD1P2) depends on the exact operating mode in use. The most important factors that affect the power consumption are: System Clock frequency, Symbol Rate, FEC type (RS or LDPC) and GPM activity (working or bypassed).

The following table contains the current consumed from the 1.2v digital core supply for several operating modes. The specified current values were measured at supply voltage of 1.2v. At a supply voltage of 1.32v the current consumption is expected to be 10% higher than specified in the table.

Table 73: Digital core current consumption for the PVG610A (and PVG610X in XPIC master mode)

SYS_CLK Frequency	Symbol Rate	With GPM LDPC	W/O GPM LDPC	With GPM RS	W/O GPM RS
200 MHz	49.5 Mbaud	3.40 A	2.85 A	2.44 A	1.92 A
	25 Mbaud	3.17 A	2.66 A	2.28 A	1.75 A
	12.5 Mbaud	2.91 A	2.54 A	1.97 A	1.58 A
	6.3 Mbaud	2.82 A	2.4 A	1.89 A	1.49 A
	3.1 Mbaud	2.75 A	2.35 A	1.85 A	1.43 A
160 MHz	40 Mbaud	2.9 A	2.48 A	2.22 A	1.81 A
	25 Mbaud	2.7 A	2.25 A	1.92 A	1.48 A
	12.5 Mbaud	2.41 A	2.12 A	1.68 A	1.34 A
	6.3 Mbaud	2.32 A	1.98 A	1.56 A	1.2 A
	3.1 Mbaud	2.28 A	1.93 A	1.51 A	1.15 A
104 MHz	25 Mbaud	2 A	1.74 A	1.45 A	1.21 A
	12.5 Mbaud	1.69 A	1.43 A	1.18 A	0.93 A
	6.3 Mbaud	1.59 A	1.36 A	1.1 A	0.84 A
	3.1 Mbaud	1.54 A	1.31 A	1.03 A	0.78 A
56 MHz	12.5 Mbaud	1 A	0.84 A	0.72 A	0.55 A
	6.3 Mbaud	0.94 A	0.79 A	0.67 A	0.51 A
	3.1 Mbaud	0.9 A	0.74 A	0.62 A	0.45 A

When using the PVG610X in slave mode the following currents are consumed. Note that at a supply voltage of 1.32v the current consumption is expected to be 10% higher than specified in the table.

Table 74: Digital core current consumption for the PVG610X in XPIC slave mode

SYS_CLK Frequency	Symbol Rate	Current consumption
200 MHz	41 Mbaud	1.31 A
	25 Mbaud	1.16 A
	13 Mbaud	1.04 A
112 MHz	25 Mbaud	0.73 A
	13 Mbaud	0.65 A

8.5.2 Digital I/O

The current consumed from VDD3P3 is calculated using the following equation:

$$I_{VDD3P3} = \sum_k \frac{V \cdot C_k \cdot F_k \cdot ActivityFactor_k}{1000}$$

Where:

- IVDD3P3 is the current drawn from VDD3P3 (in mA)
- Summing is performed over all the output pins being used in the application
- V is the voltage of VDD3P3 (in volts)
- Ck is the load capacitance of the kth output pin (in pF)
- Fk is the frequency of the kth output pin (in MHz)
- ActivityFactork is the percentage of data toggling of the kth output pin

For example: the 8 Rx_data pins of the GPI, running at a frequency of 50MHz, with a load of 15pF, at 3.3v, will consume: 8*3.3*15*50*0.5/1000=9.9mA

8.5.3 LIU

The current consumed from the LIU supply (LIU_VDD3P3) depends on the number of PDH links in use.

Table 75: LIU current consumption

Parameter	Value
Idle current (non of the LIU ports is in use)	125mA
Current consumed by any additional LIU port	35mA

Note the following:

- The specified current values were measured at supply voltage of 3.3v. At a supply voltage of 3.6v the current consumption is expected to be 10% higher than specified above.
- The current consumption for active LIU ports was measured for transmission of random data. When transmitting AIS signal (all ‘ones’), the current consumption is increased to 48ma.
- When connecting E1/T1 line to the PVG610, some of the power is transferred to the line. For example, a 120ohm E1 line consumes ~37.5mw. This power is not dissipated inside the PVG610A and thus it should be subtracted from the consumed power when performing thermal analysis.
- When using devices with manufacturing part numbers 'EC261752B-1N-1' (for PVG610) or 'EC261752B-2N-1' (for PVG610X), the idle current is 205ma.

Systems not using PDH or XPIC functionality can connect lower voltage level to the LIU_VDD3P3 pin. The lowest allowed voltage level depends on the level driving the LVPECL levels of SYS_CLK as follows:

Min(LIU_VDD3P3)=Vcc(LVPECL)-2v

For Vcc(LVPECL) in the range of 3-3.6v, the LIU_VDD3P3 is in the range of 1-1.6v. Within this range the idle power consumption is reduced compared to using 3.3v.

8.5.4 AFE

8.5.4.1 Dual 12-bit ADC

Table 76: Dual 12-bit ADC current consumption

Parameter	Value
1.2v supply Current (ADC_VDD1P2 and ADC_CLK_VDD1P2 pins)	47mA+0.83mA*SamplingFrequency
3.3v supply Current	10mA

The specified current values were measured at supply voltage of 1.2 and 3.3v. At a supply voltages of 1.32v and 3.6v, the current consumptions are expected to be 10% higher.

8.5.4.2 IF Sampling 10-bit ADC

Table 77: IF sampling 10-bit ADC current consumption

Parameter	Value
1.2v supply Current (ADC_VDD1P2 and ADC_CLK_VDD1P2 pins)	0.3mA*SamplingFrequency
3.3v supply Current (ADC_VDD3P3 pin)	5mA

The specified current values were measured at supply voltage of 1.2 and 3.3v. At a supply voltages of 1.32v and 3.6v, the current consumptions are expected to be 10% higher.

8.5.4.3 Dual 12-bit DAC

Table 78: Dual 12-bit DAC current consumption

Parameter	Value
1.2v supply Current (DAC_VDD1P2 and DAC_CLK_VDD1P2 pins)	0.07mA*SamplingFrequency
3.3v supply Current (DAC_VDD3P3 pin)	60mA

The specified current values were measured at supply voltage of 1.2 and 3.3v. At a supply voltages of 1.32v and 3.6v, the current consumptions are expected to be 5% and 10% higher respectively.

8.5.4.4 Envelope 10-bit ADC

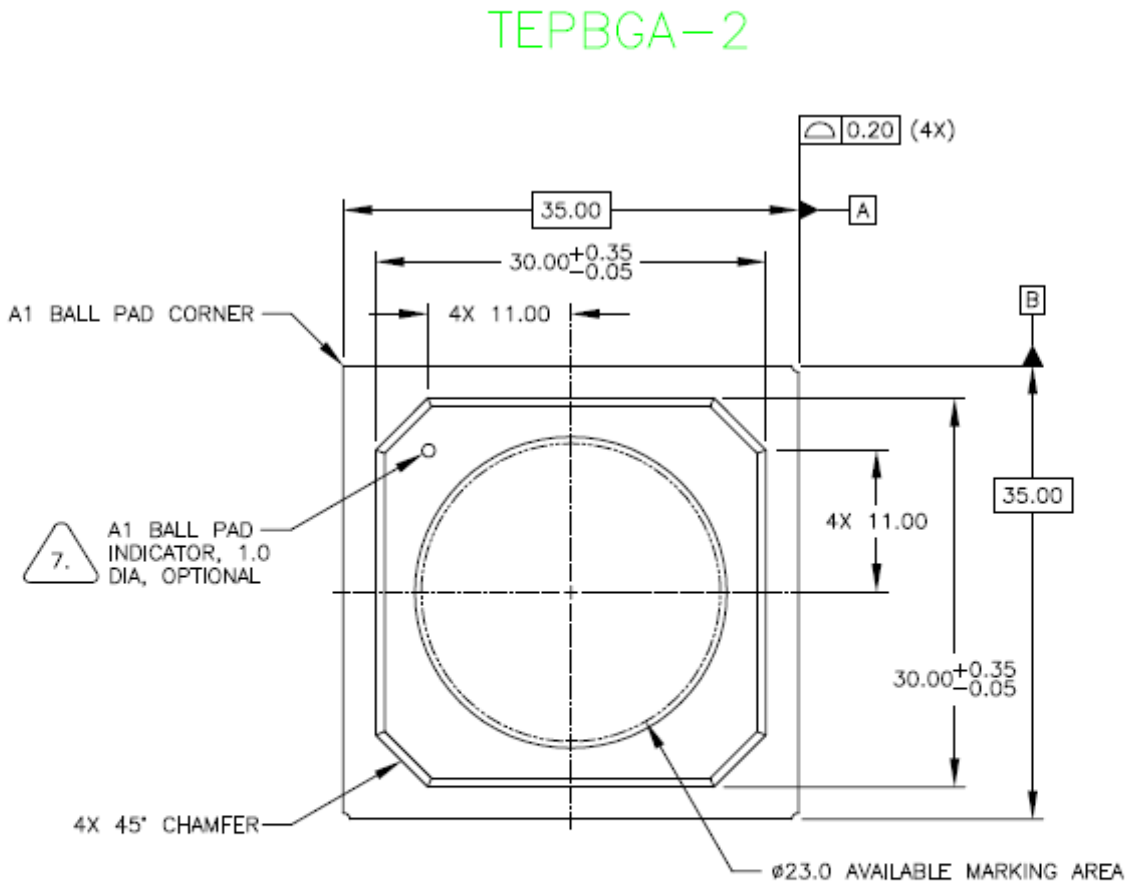
Table 79: Envelope 10-bit ADC current consumption

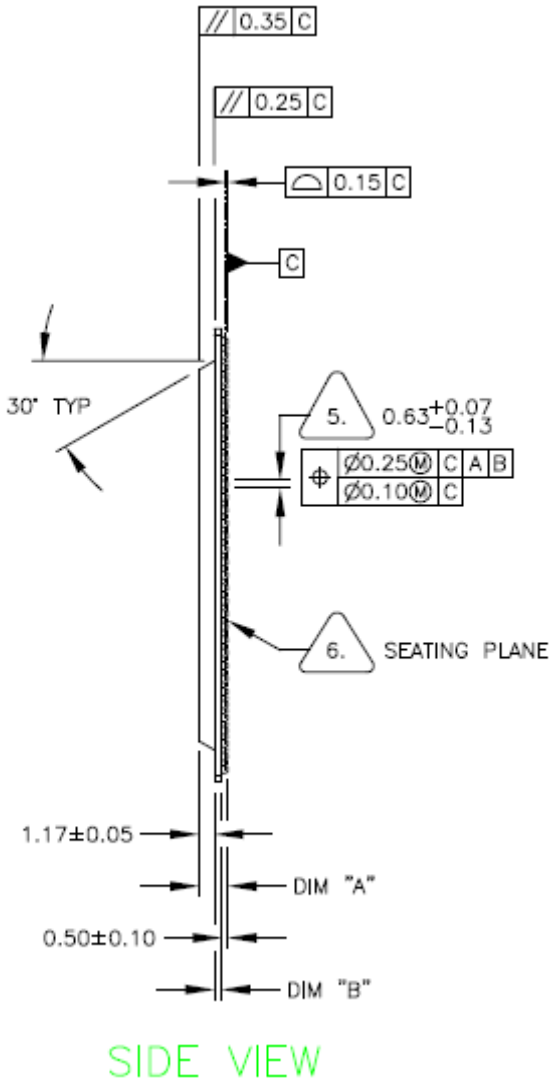
Parameter	Value
1.2v supply Current (DAC_VDD1P2 pin)	11mA+0.27mA*SamplingFrequency

The specified current values were measured at supply voltage of 1.2v. At a supply voltages of 1.32v, the current consumption is expected to be 10% higher.

9 Packaging

9.1 Dimensions





4	2.23±0.21	0.56±0.006	STANDARD
NO. LAYERS	DIM “A”	DIM “B”	NOTES
TEPBGA-2 THICKNESS SCHEDULE			

Figure 117: 680 Ball POD Dimensions

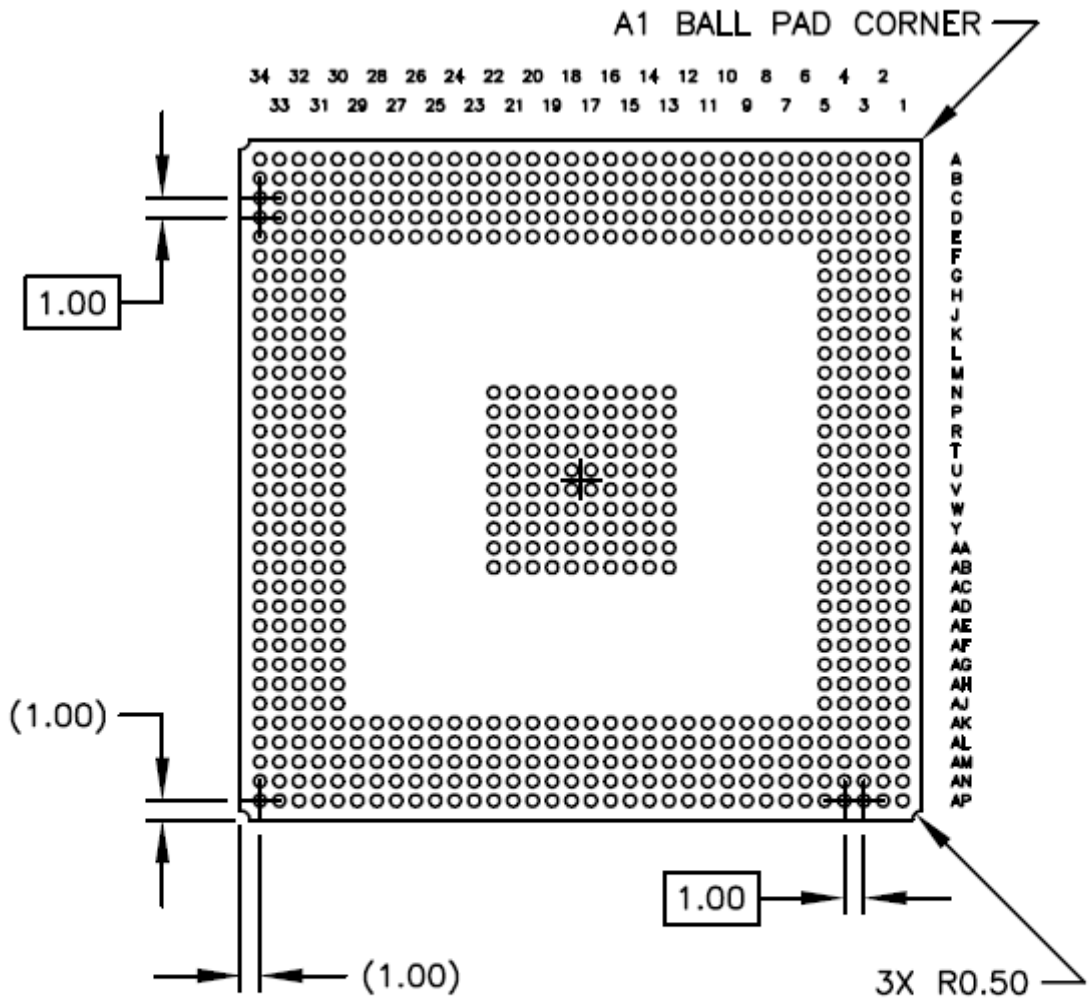


Figure 118: 680 Ball POD Bottom View

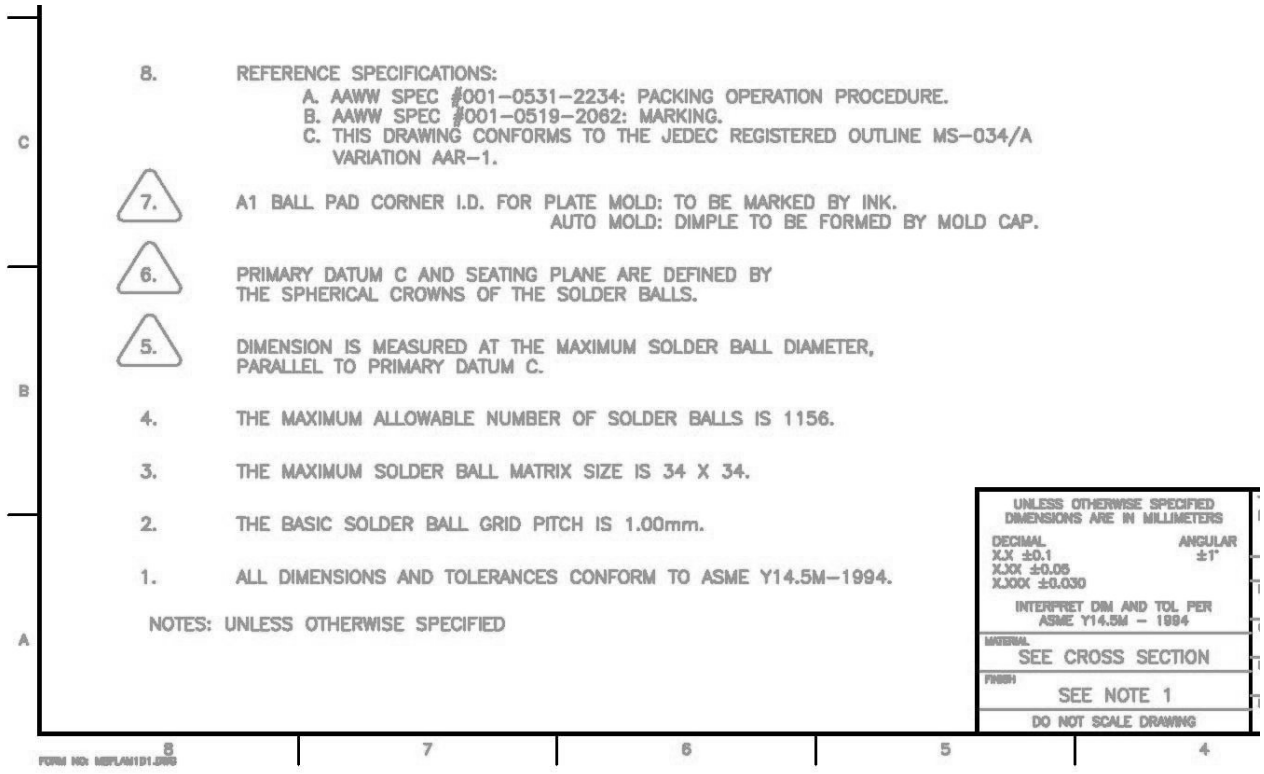


Figure 119: Packaging Notes From mechanical Drawing

9.2 Thermal Parameters

Junction to Case Resistance	Θ_{JC}	3.1°C/W
Junction to Ambient Resistance	Θ_{JA}	12.2°C/W
Junction Temperature	TJ	-40 to 125°C
Storage Temperature	T_{STG}	-40 to 150°C

9.3 Lead Free

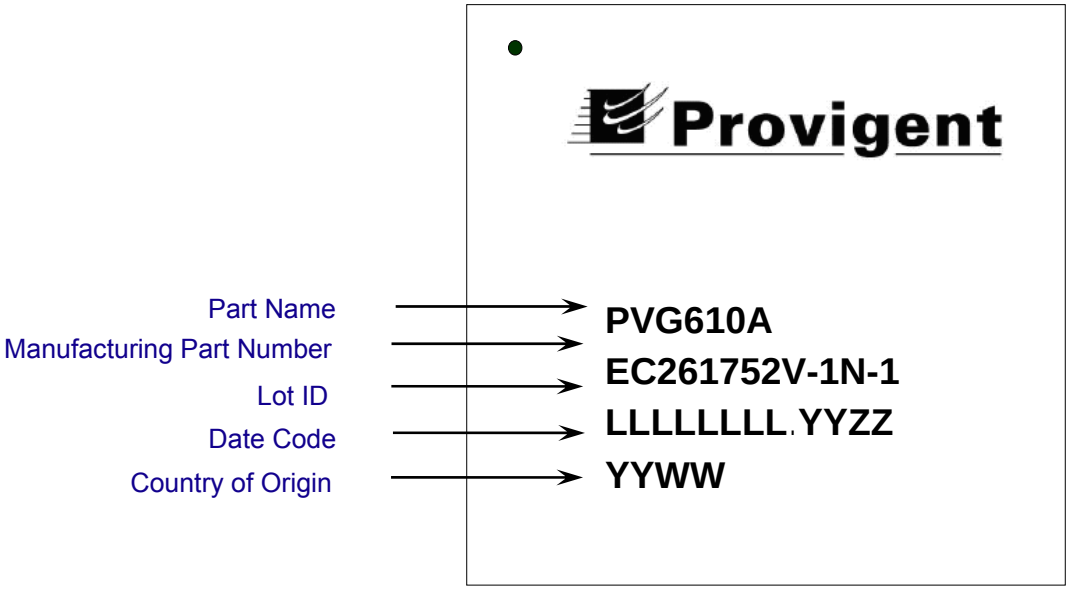
The PVG610A is in compliance with the European Union's Restriction of Hazardous Substances (RoHS) legislation.

9.4 Soldering

Soldering of the device should be in accordance to JEDEC J-STD-020D (for pb-free packages). The allowed peak temperature is 260°c. The Moisture Sensitivity Level (MSL) of the device is Level 3.

9.5 Packaging Marking

9.5.1 PVG610A Marking



Note that 'V' in the Manufacturing part number is hardware revision number. See the errata doc for available revisions and the difference between them.

9.5.2 PVG610X Marking

Part Name: PVG610X

Manufacturing Part Number: EC261752V-2N-1

Note that 'V' in the Manufacturing part number is hardware revision number. See the errata doc for available revisions and the difference between them.

10 Ordering Information

Part Name	Ordering Number
PVG610	0610-050-000-008
PVG610X	0610-050-002-006

11 Glossary of Terms

Acronym	Description
ACI	Adjacent-Channel Interference
ACM	Adaptive Code Modulation
ADC	Analog to Digital Converter
AFE	Analog Front End
AGC	Automatic Gain Control
AIS	Alarm Indication Signal
ATPC	Automatic Transmit Power Control
AWGN	Additive White Gaussian Noise
BER	Bit Error Rate
BIP	Bit Interleaved Parity
BPSK	Bi-polar Phase Shift Key
CAS	Channel Associated Signaling
CCI	Co-Channel Interference
CMA	Constant Modulus Algorithm
CoA	Class of Availability
DAC	Digital to Analog Converter
DCC	Data Communication Channel
DCE	Data Communication Equipment
DTE	Data Terminal Equipment
EOW	Engineering Order Wire
FDD	Frequency Division Duplex
FDF	Fractionally Delay Filter
FEC	Forward Error Correction
FFF	Feed Forward Filter
FPA	Fast Preamble Acquisition
GPI	General Purpose Interface
GPIO	General Purpose Input/Output
GPM	General Purpose Multiplexer
LDPC	Low Density Parity Check
LDPC	Low-Density Parity Check
LIU	Line Interface Unit
LOF	Loss of Frame
LOS	Loss of Signal
LVCMOS	Low Voltage CMOS
MII	Media Independent Interface
MSE	Mean Square Error
NOF	Number of Frames
OMI	Outband Management Interface
OOF	Out of Frame

Acronym	Description
PHY	Physical Layer Interface
PRBS	Pseudo-Random Bit Sequence
QAM	Quadrature Amplitude Modulation
QPSK	Quadrature Phase Shift Keying
RDI	Remote Fault Indication
RS	Reed Solomon
RSSI	Receive Signal Strength Indication
Rx	Receive
SERDES	Serialize Deserialize
SNR	Signal-to-Noise Ratio
SPA	Slow Preamble Acquisition
TDD	Time Division Duplex
TIM	Trace Identifier Mismatch
TOH	Transport Overhead
Tx	Transmit
WD	Watchdog
XPIC	Cross Polarization Interference Cancellation